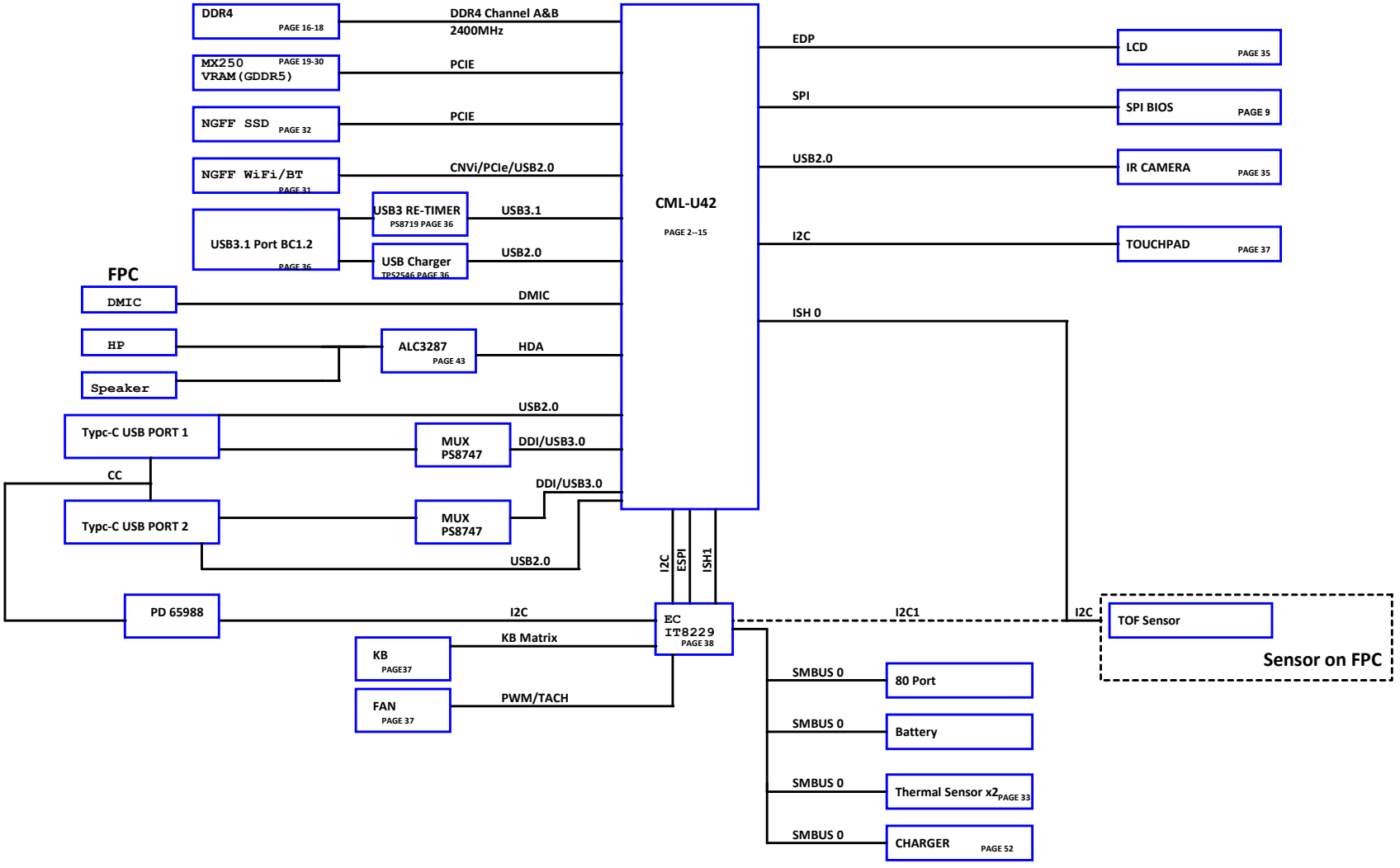
S540-13 CML-U42/v1 Schematic Block Diagram



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Title: CML Block Diagram		
Size: C	Document Number: S540-13	Rev: V0.5
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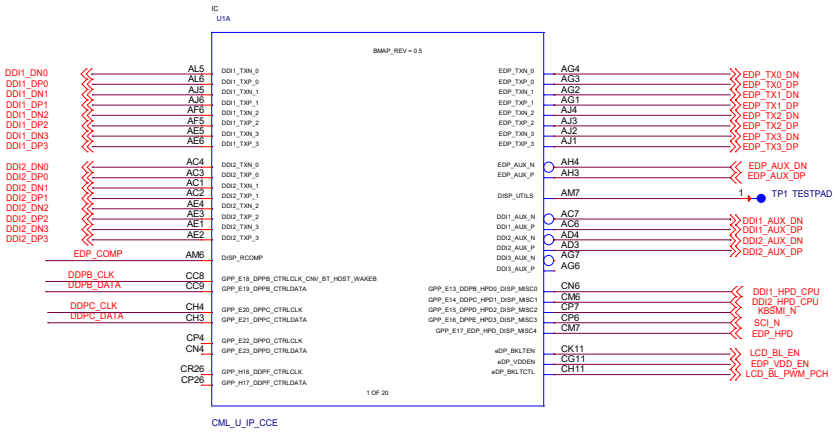

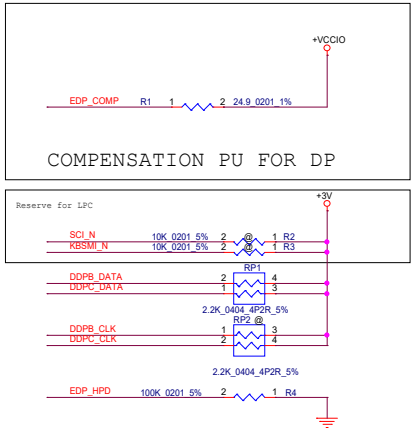

Table 53. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	

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Title: CML MCP (DDI,EDP)

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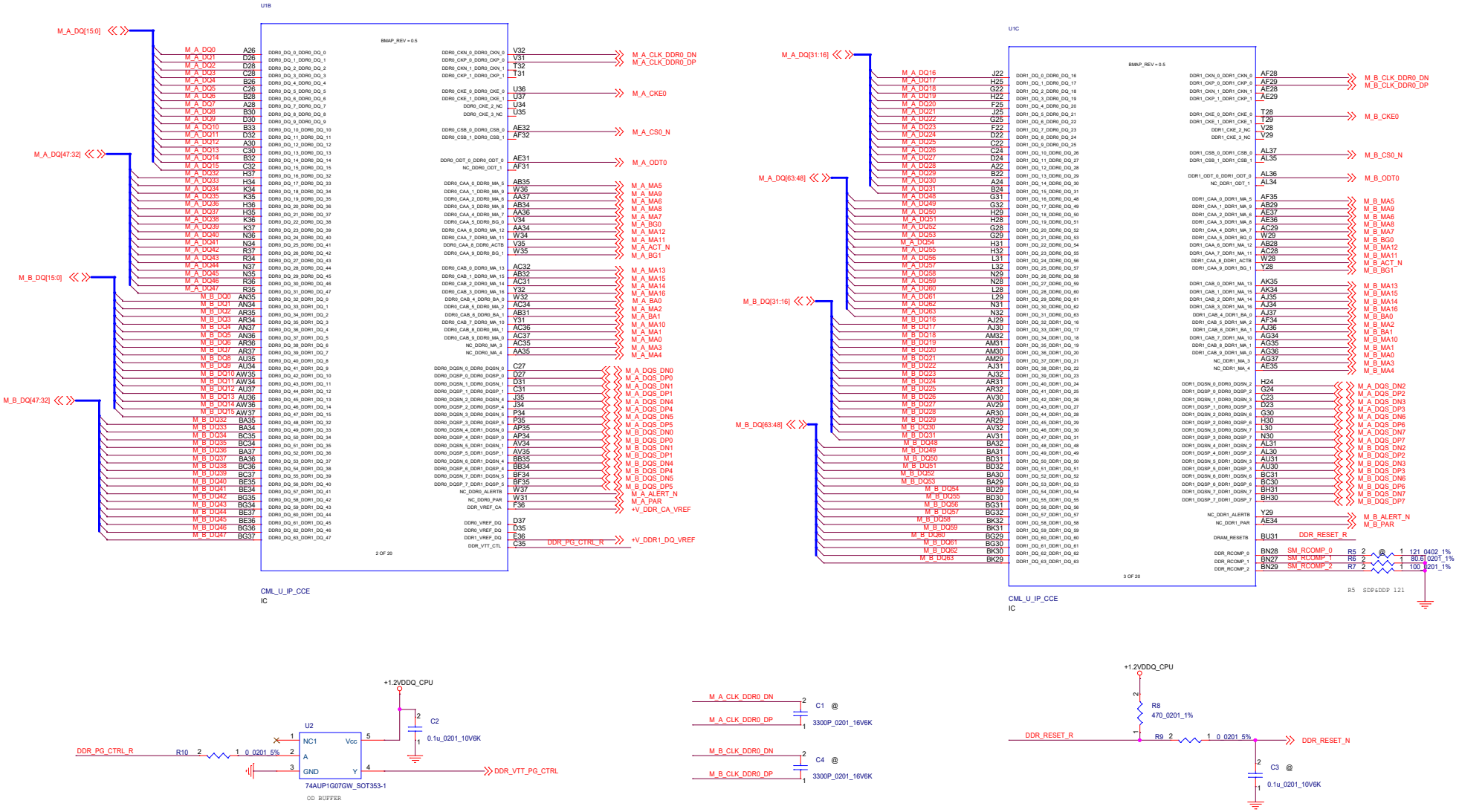

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Title: CML MCP (PROCESSOR DDR4)

Size	Document Number	Rev
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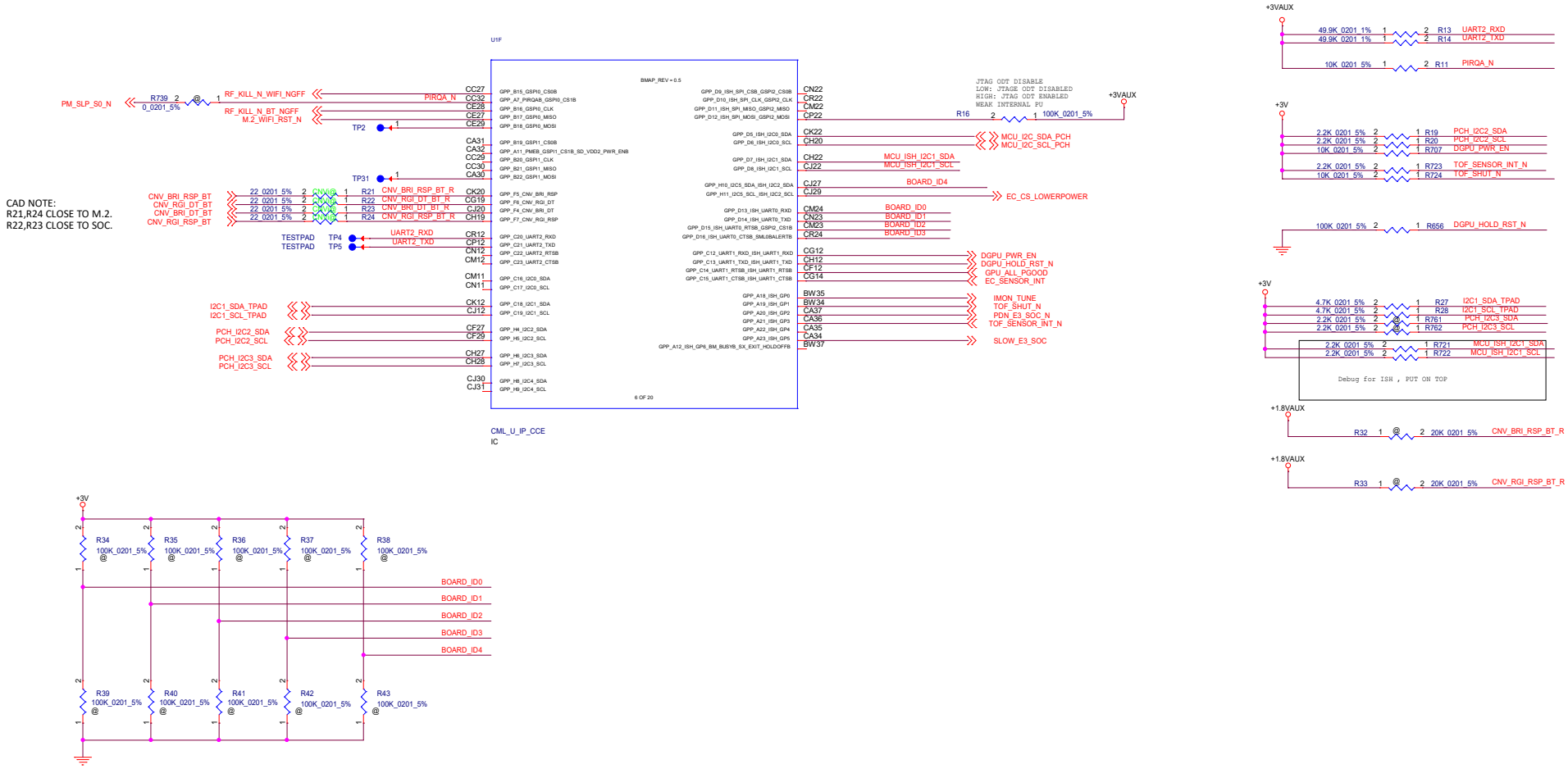

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Title: CML MCP (PCH GPIO)		
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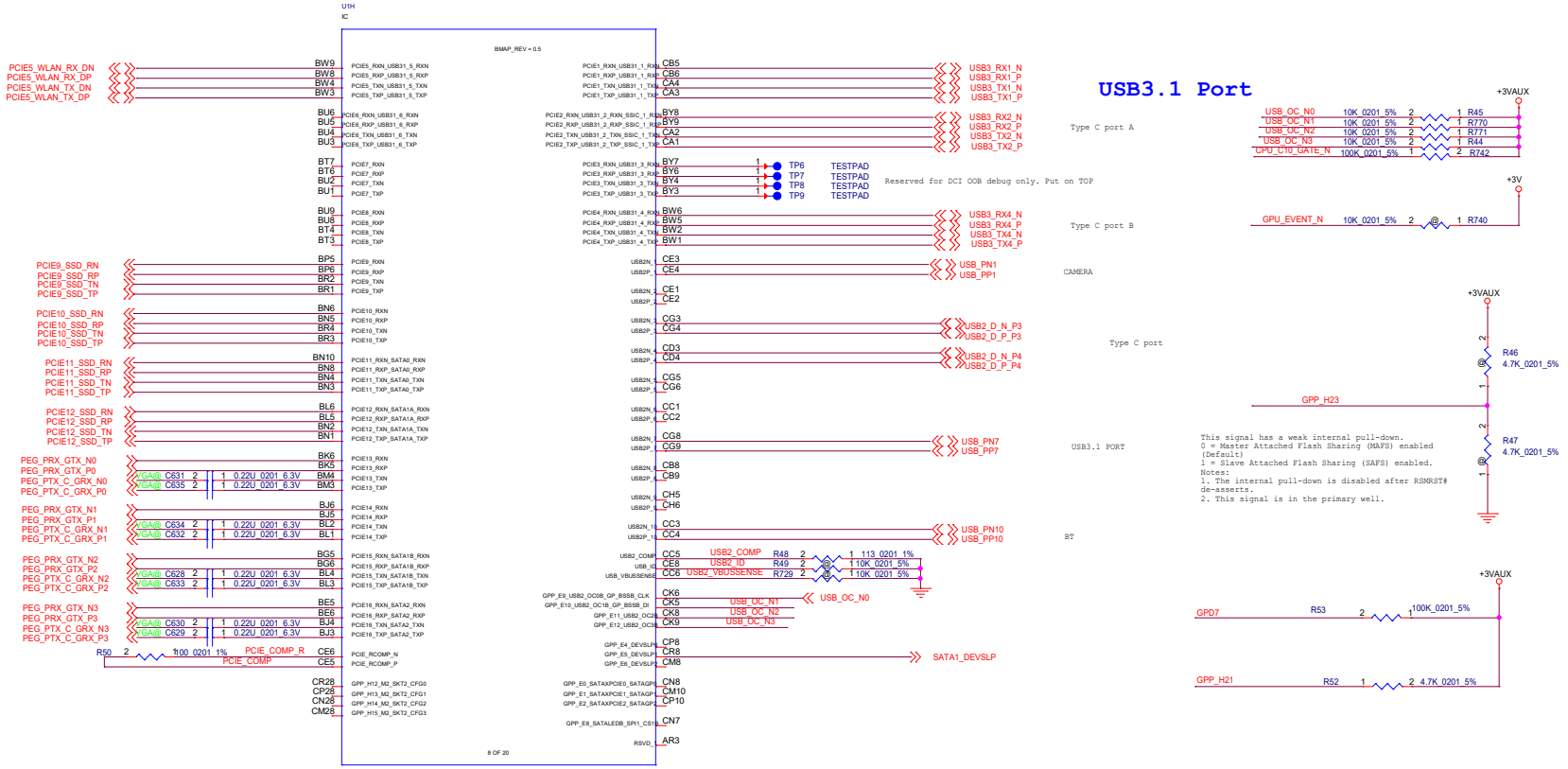
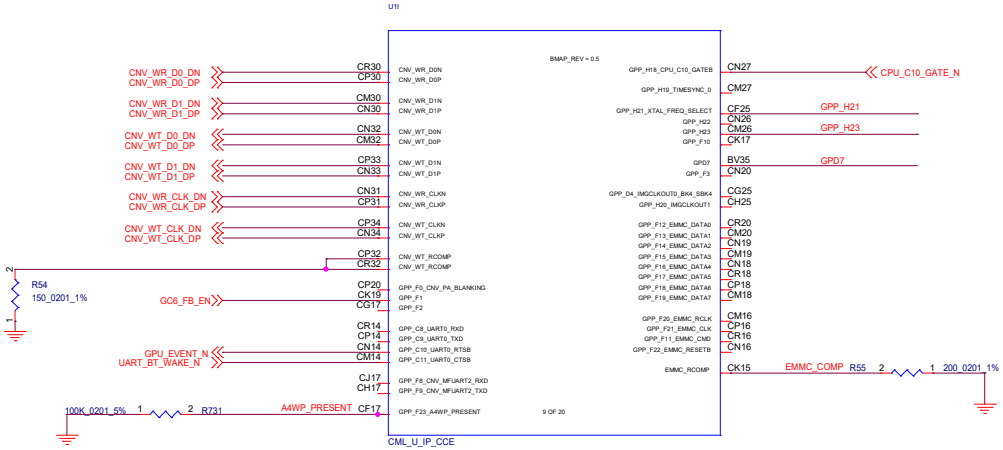
Wlan

PCIE Port 9-Port 11 SSD

PCIE Port 13-Port 16 GPU

USB3.1 Port





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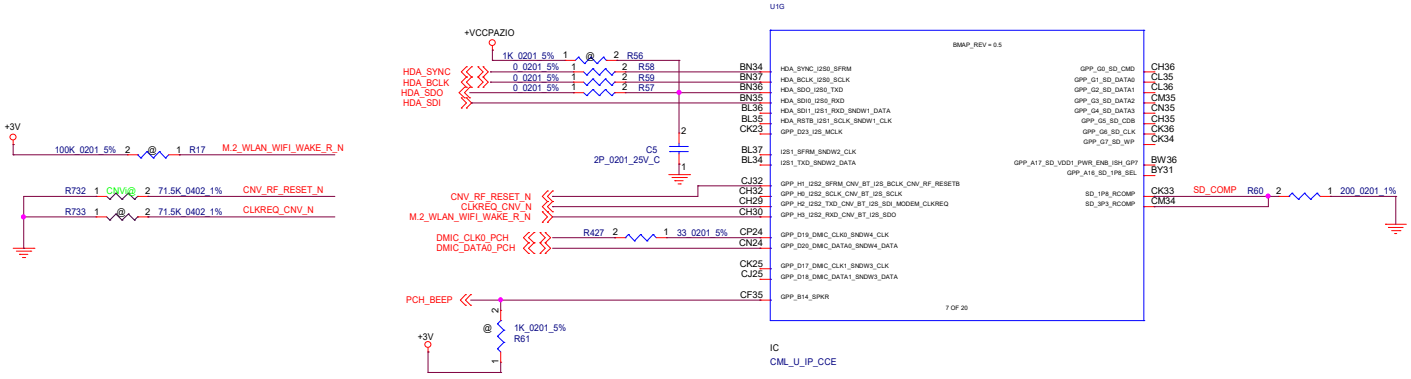

lenovo联想	LENOVO.CRDN	
Title	CML MCP (HDA/I2S/SDIO/DMIC)	
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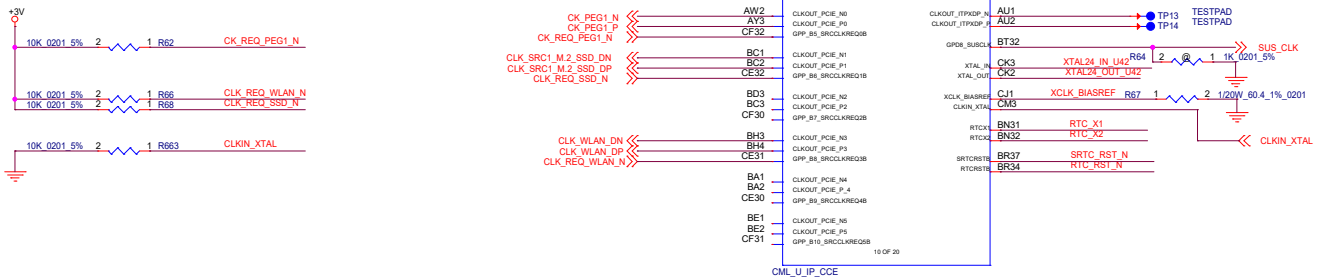
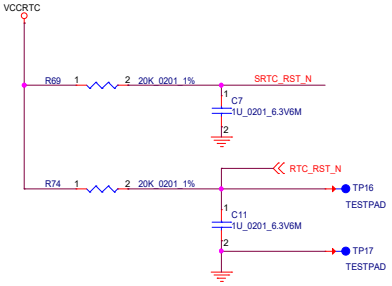
Any un-used SRCCLKRQ# signal not mapped to a Down Device or Connector/ADD-in Card must be disabled using the Kaby Lake Platform FITC tool and they must be left as no connects at the CPU side on the platform

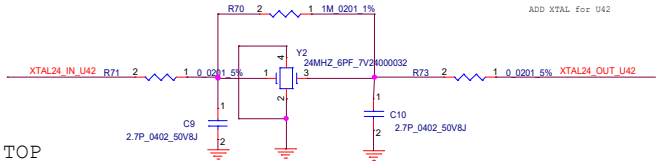


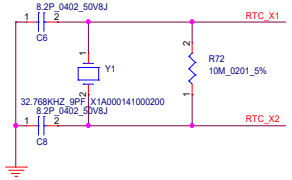


ME RESET
SAVE ME = PU (Default)
CLEAR ME = PD

CMOS RESET
SAVE CMOS = PU (Default)
CLEAR CMOS = PD

TP16 TP17 Need to put on the TOP





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Title: CML MCP (CLK)

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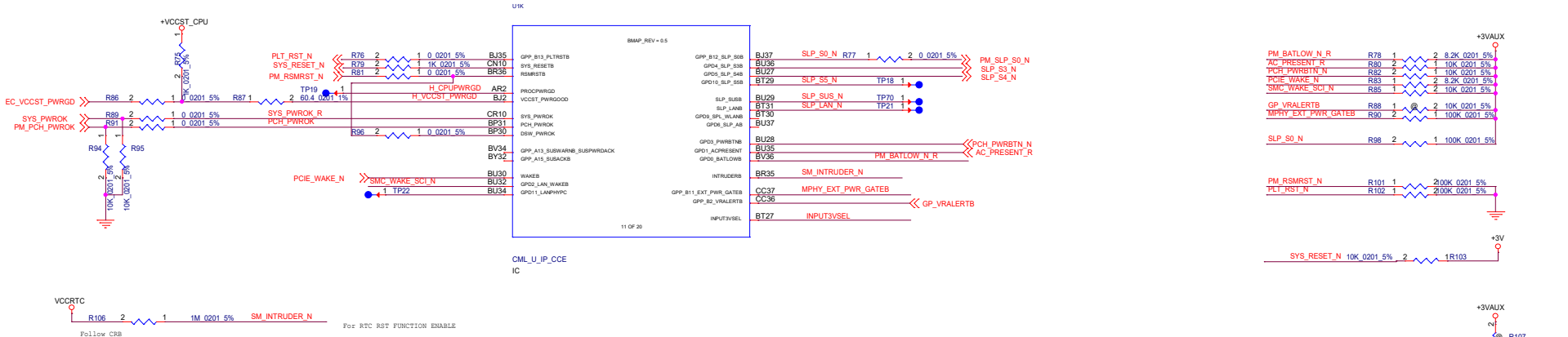
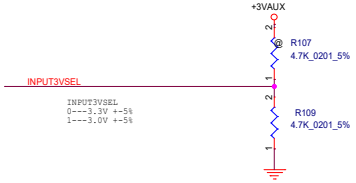


CML_U_IP_CCE

IC



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Title: CML MCP (PM)

Size: C | Document Number: S540-13 | Rev: V0.5

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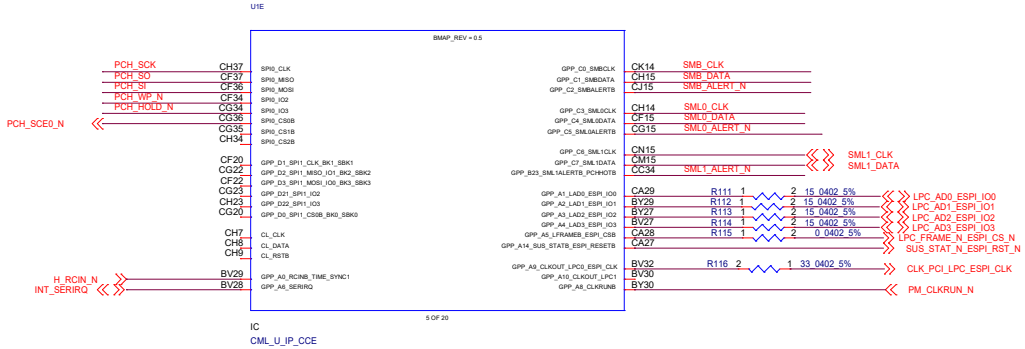
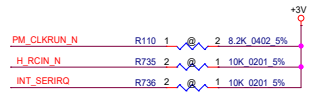
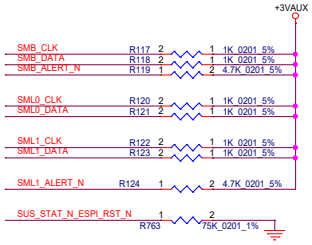
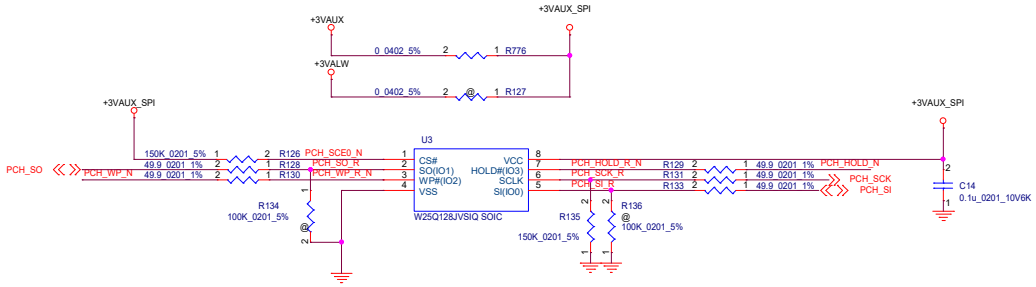


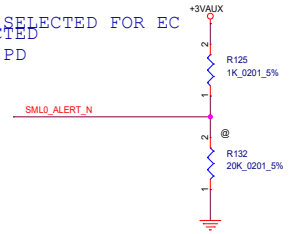
IC
CML_U_IP_CCE

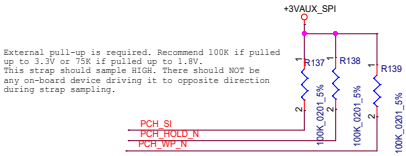






SML0_ALERT_N
HIGH: ESPI IS SELECTED FOR EC
LOW: LPC SELECTED
WEAK INTERNAL PD





External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

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Title: CML MCP (eSPI SPI SMB CLINK)

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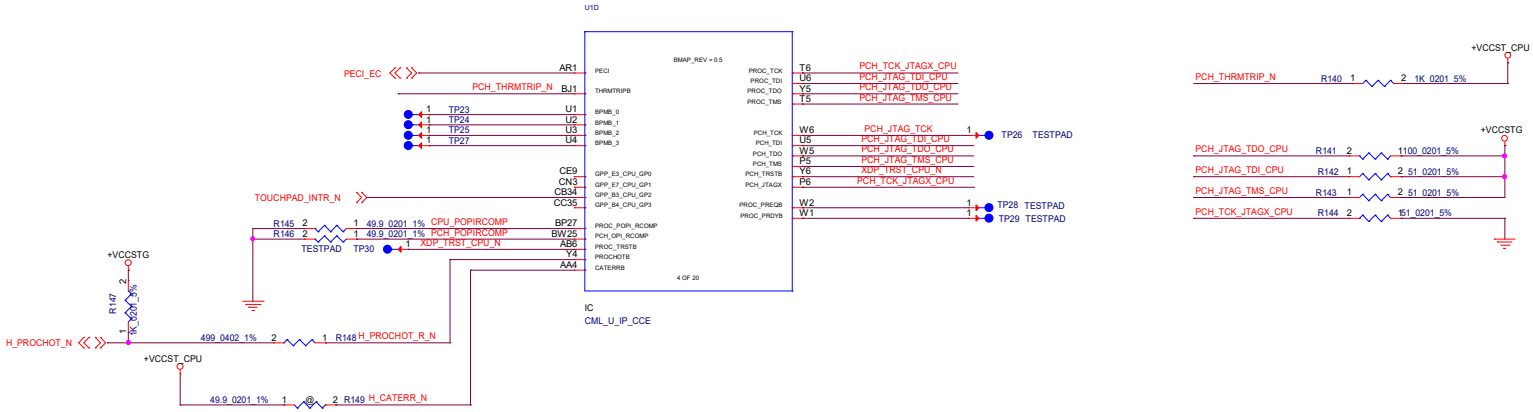

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Title: CML MCP (MISC JTAG)		
Size: C	Document Number: S540-13	Rev: V0.5
Date: Monday, June 17, 2019	Sheet 10 of 63	

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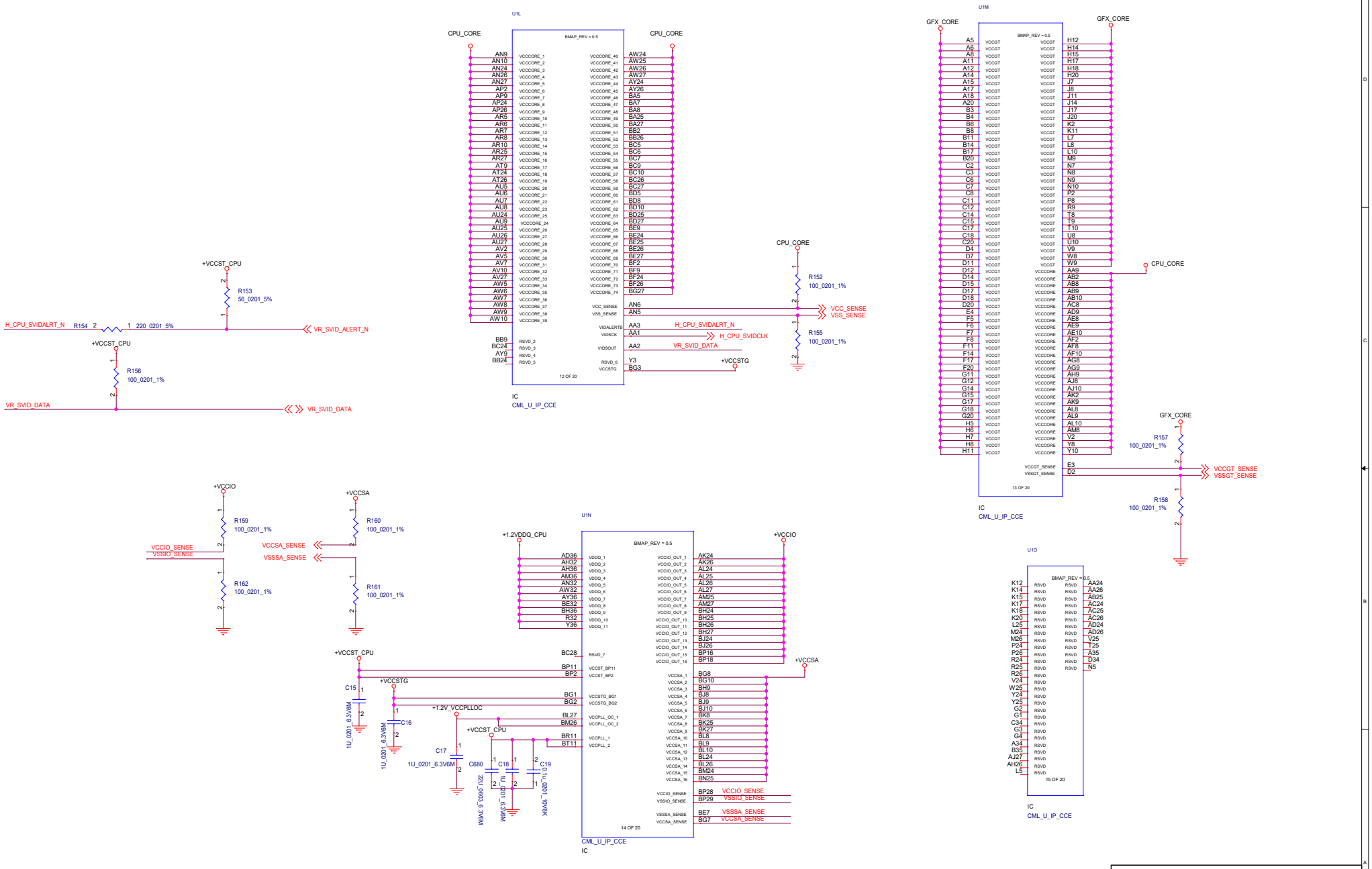

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Title: CML MCP (PROCESSOR POWER)

Size	Document Number	Rev
C	S540-13	V0.5

Date: Monday, June 17, 2019 Sheet 11 of 63

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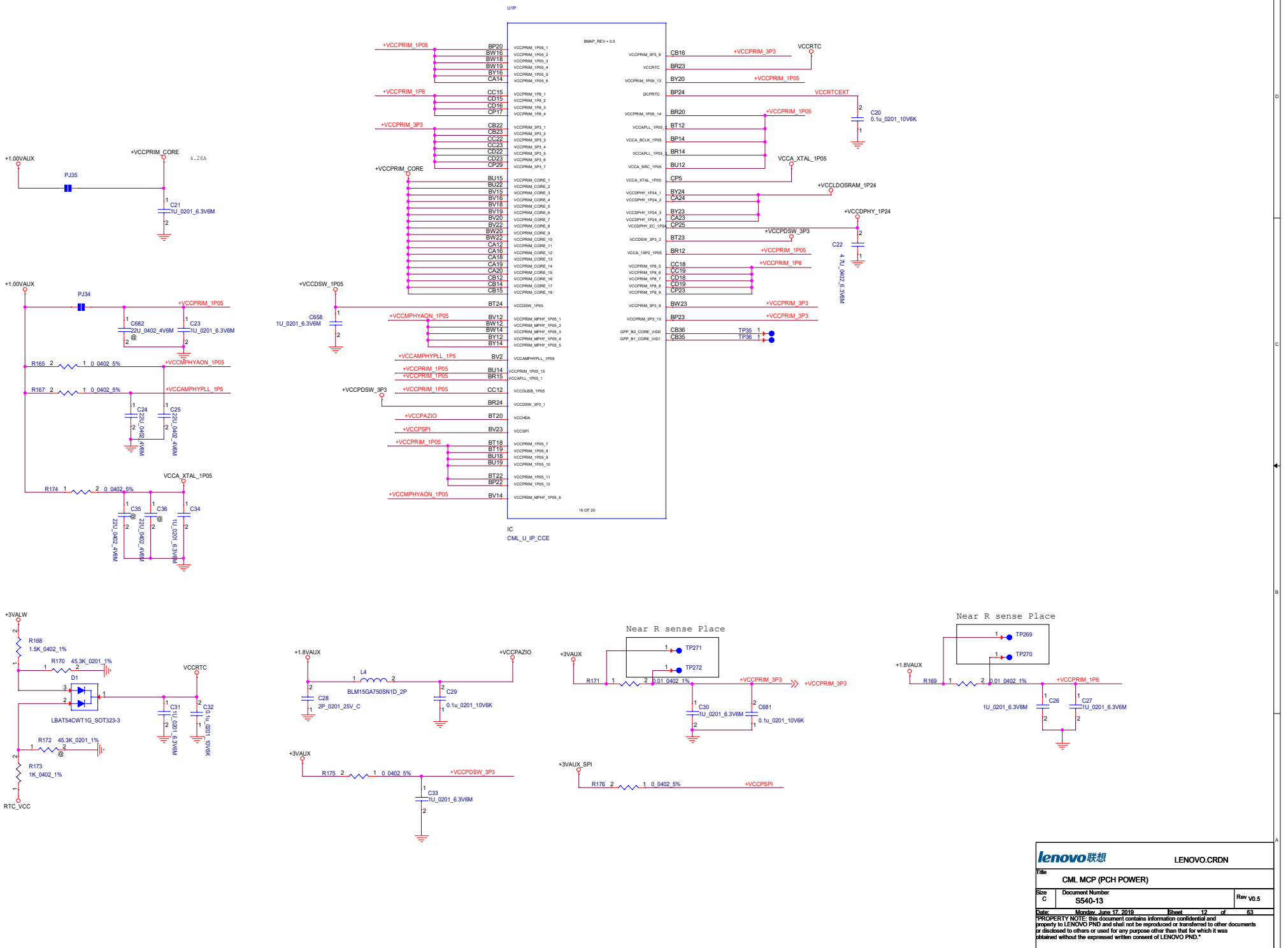

lenovo联想	LENOVO.CRDN
Title	CML MCP (PCH POWER)
Size C	Document Number S540-13
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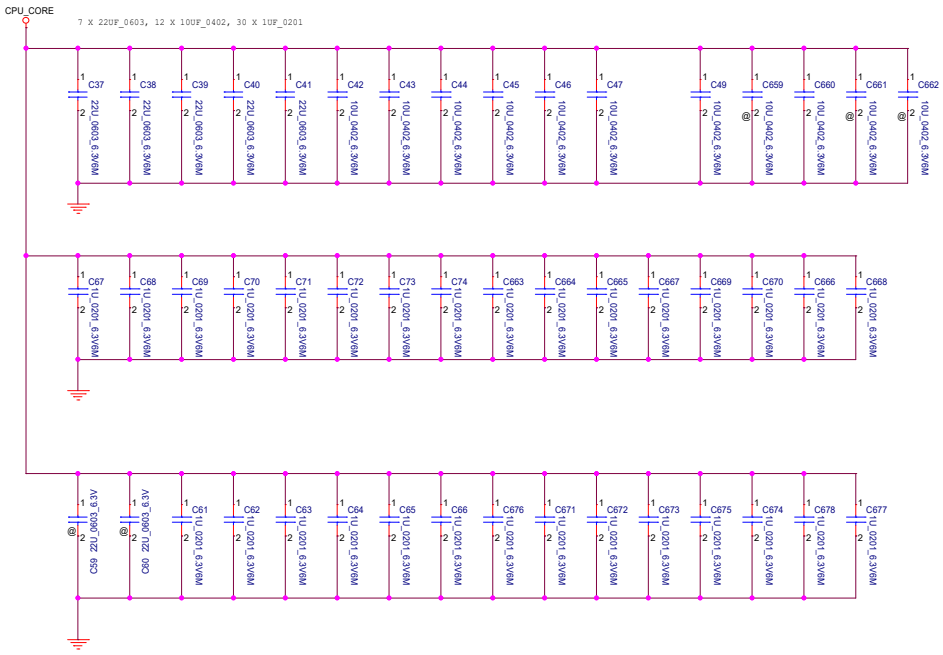

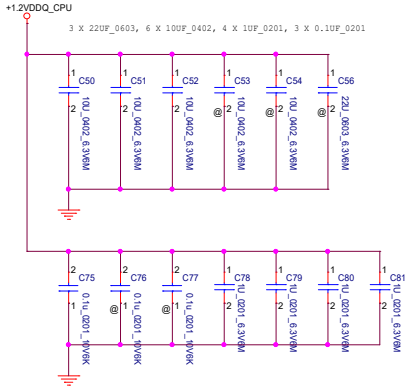

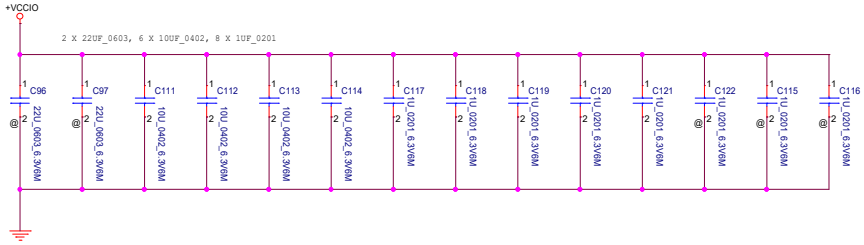

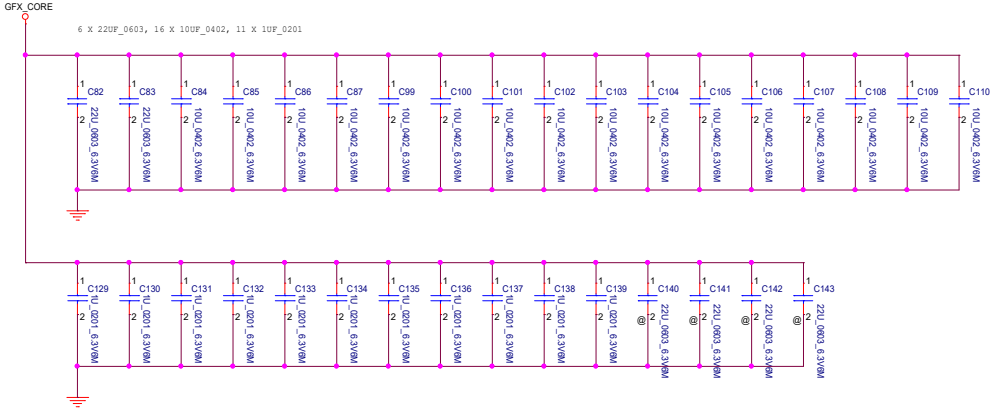

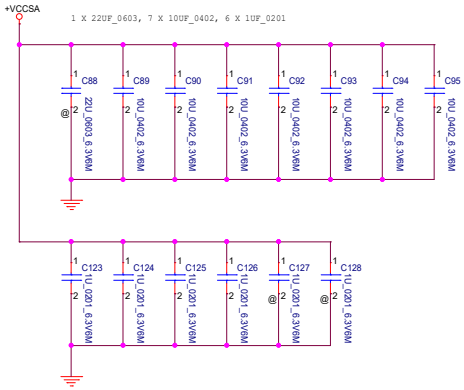

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Title: CML MCP (Power CAP)

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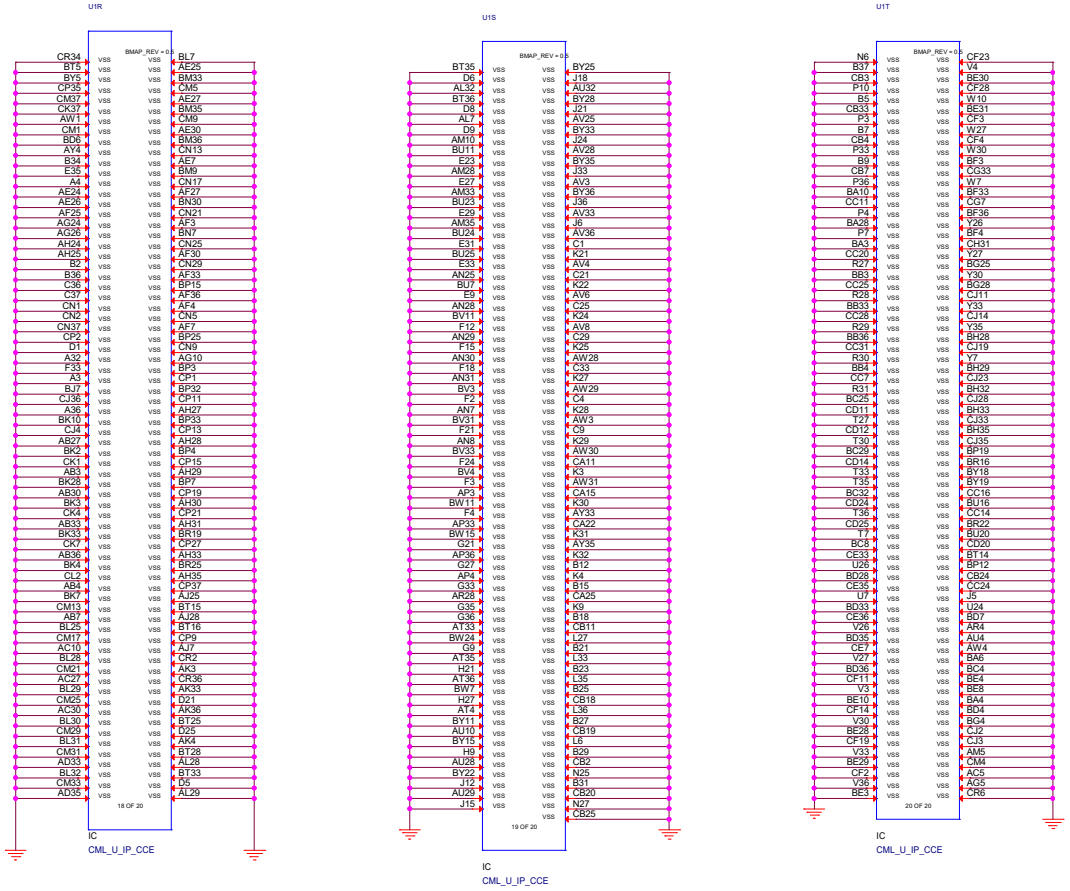

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Title: CML MCP (GND)

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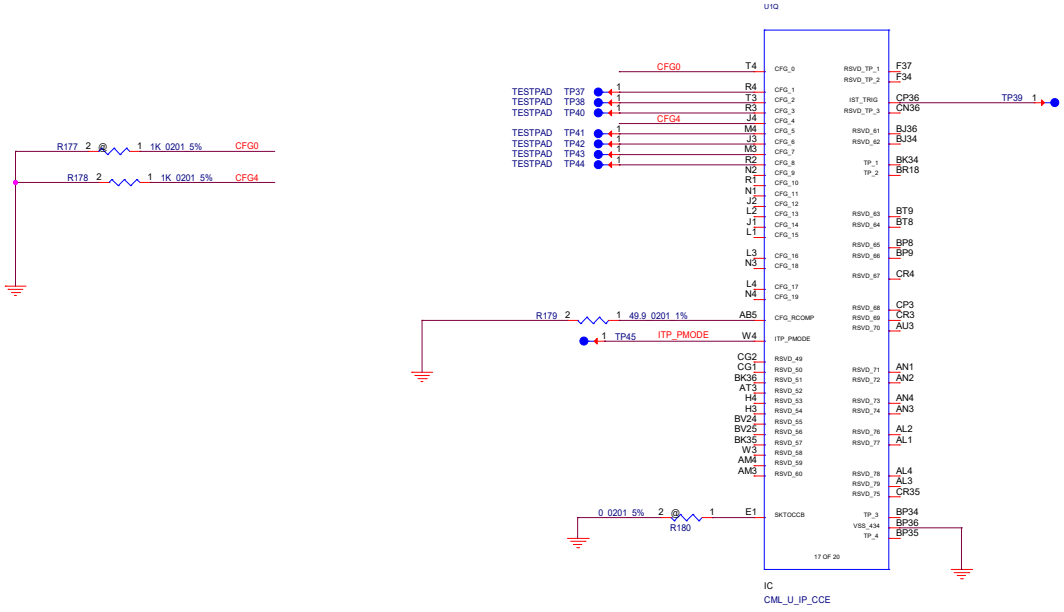

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Title: CML MCP (RSVD)		
Size: C	Document Number: S540-13	Rev: V0.5
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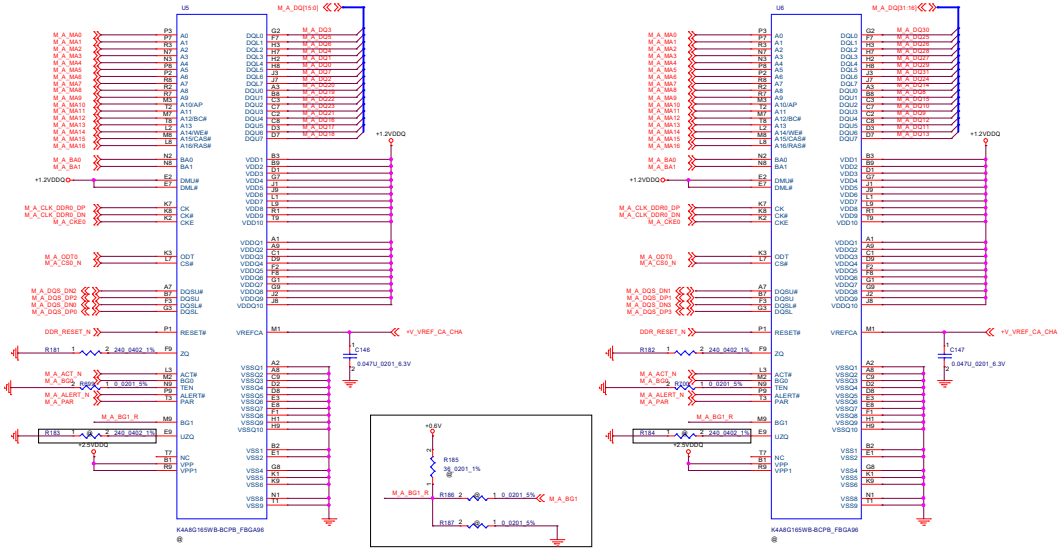
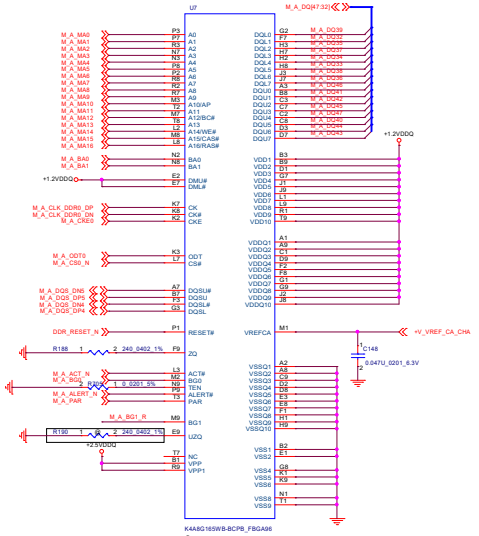
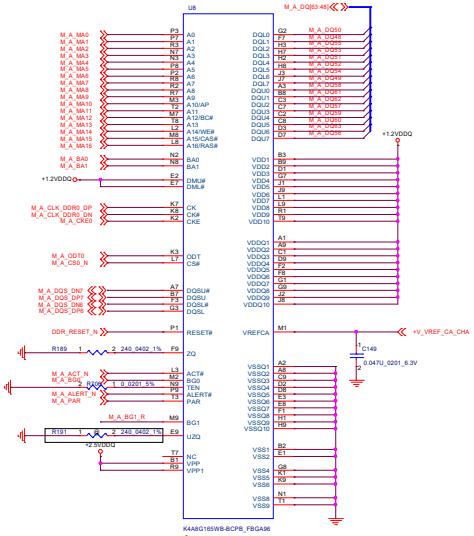


DDP: Stuff R186 and R185, Dummy R187; R183 184 190 191 @ 240ohm
SDP: Dummy R186 and R185, Stuff R187; R183 184 190 191 @ 0ohm





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Title: DDR4-CHA ONBD		
Size: D	Document Number: S540-13	Rev V0.5
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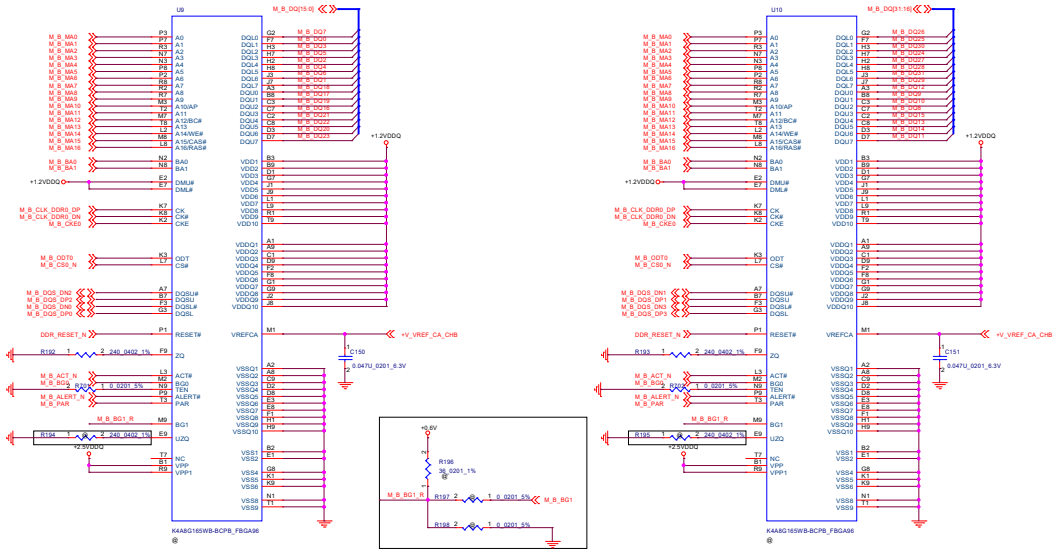
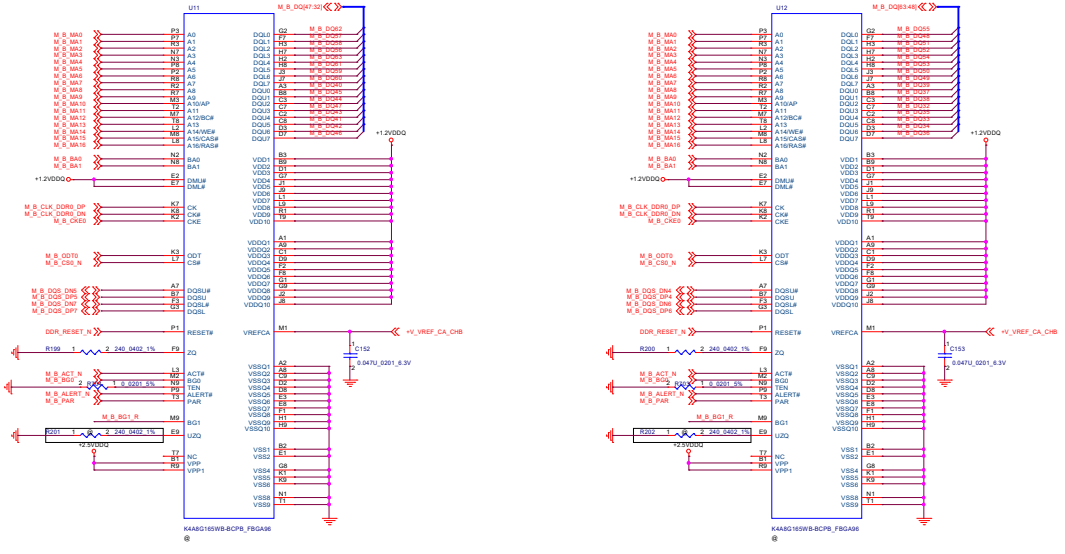


DDP: Stuff R197 and R196, Dummy R198; R194 195 201 202 @ 240ohm
SDP: Dummy R197 and R196, Stuff R198; R194 195 201 202@ 0ohm



lenovo 联想		LENOVO.CRDN	
Title: DDR4-CHB ONBD			
Size: D	Document Number: S540-13		Rev V0.5
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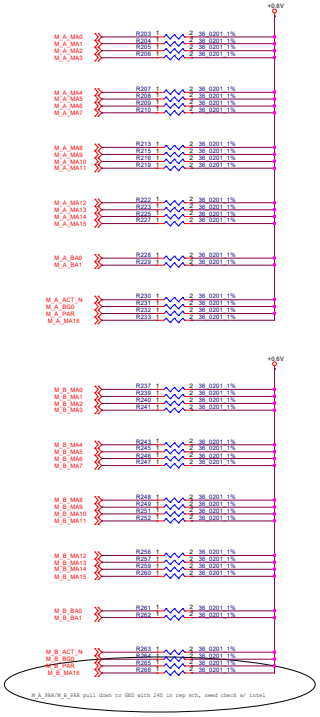

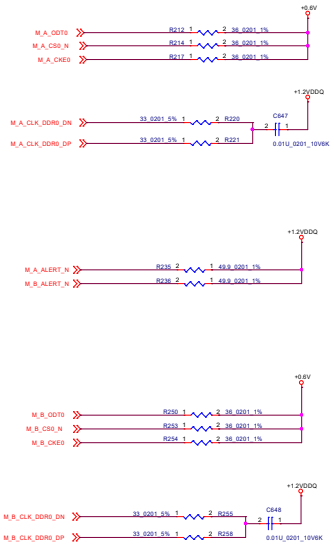

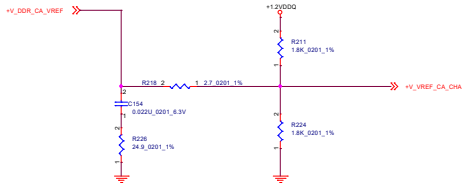

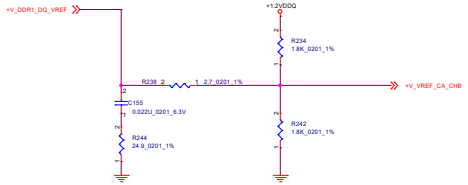

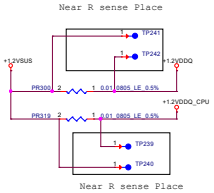

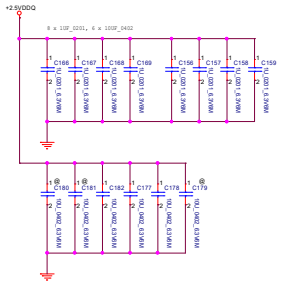

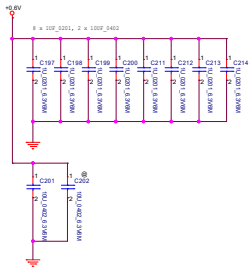

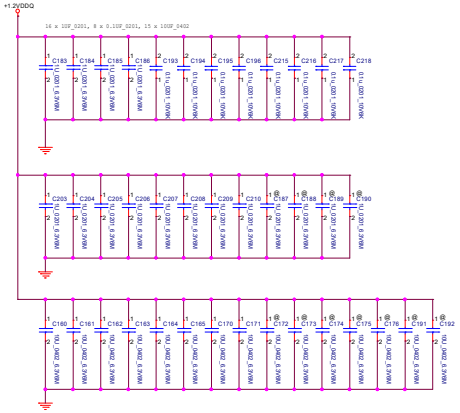

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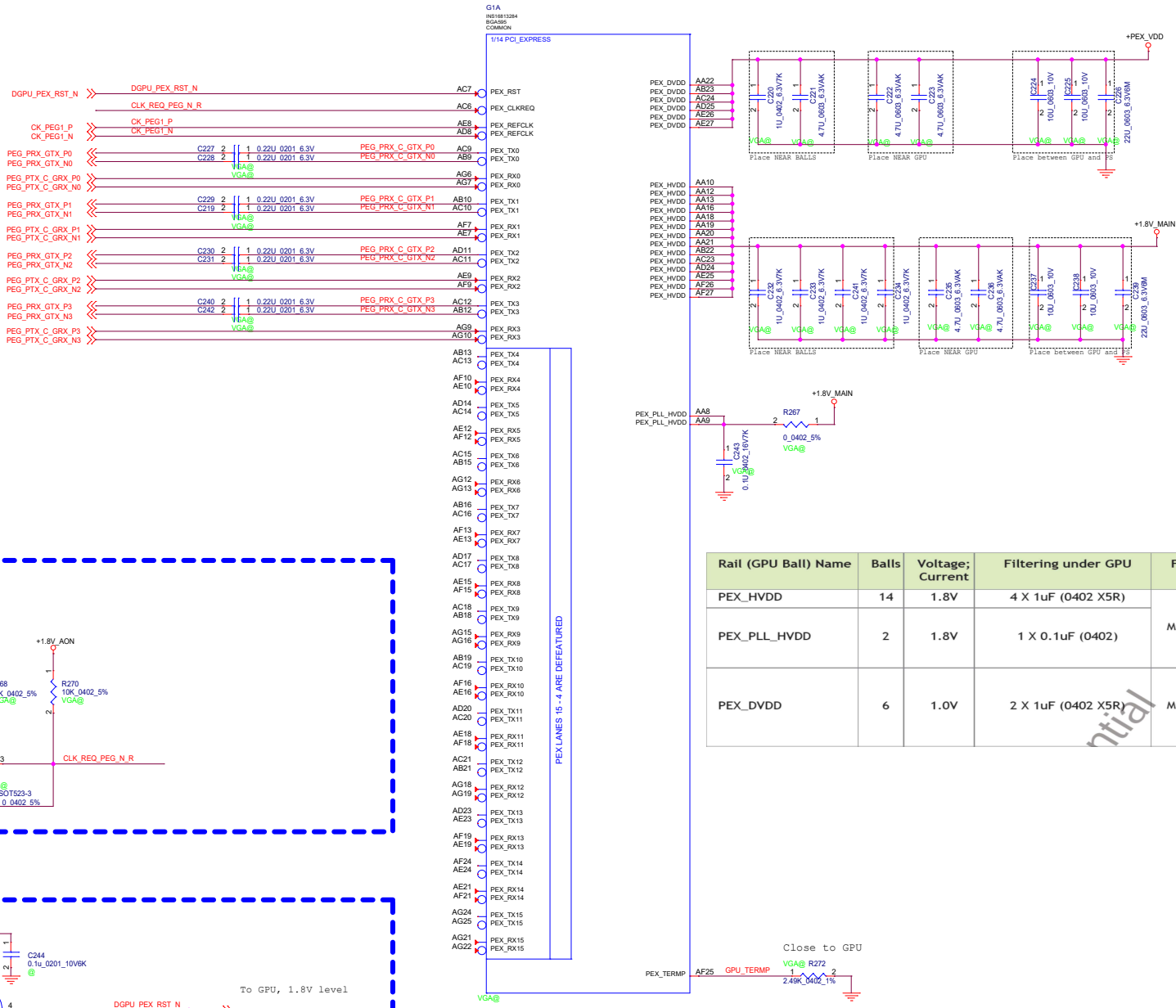
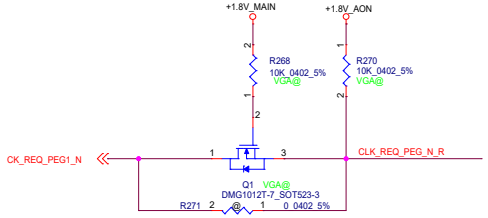
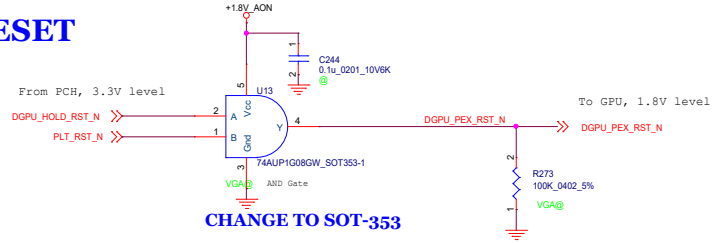


Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)

CLK_REQ_N



GPU RESET



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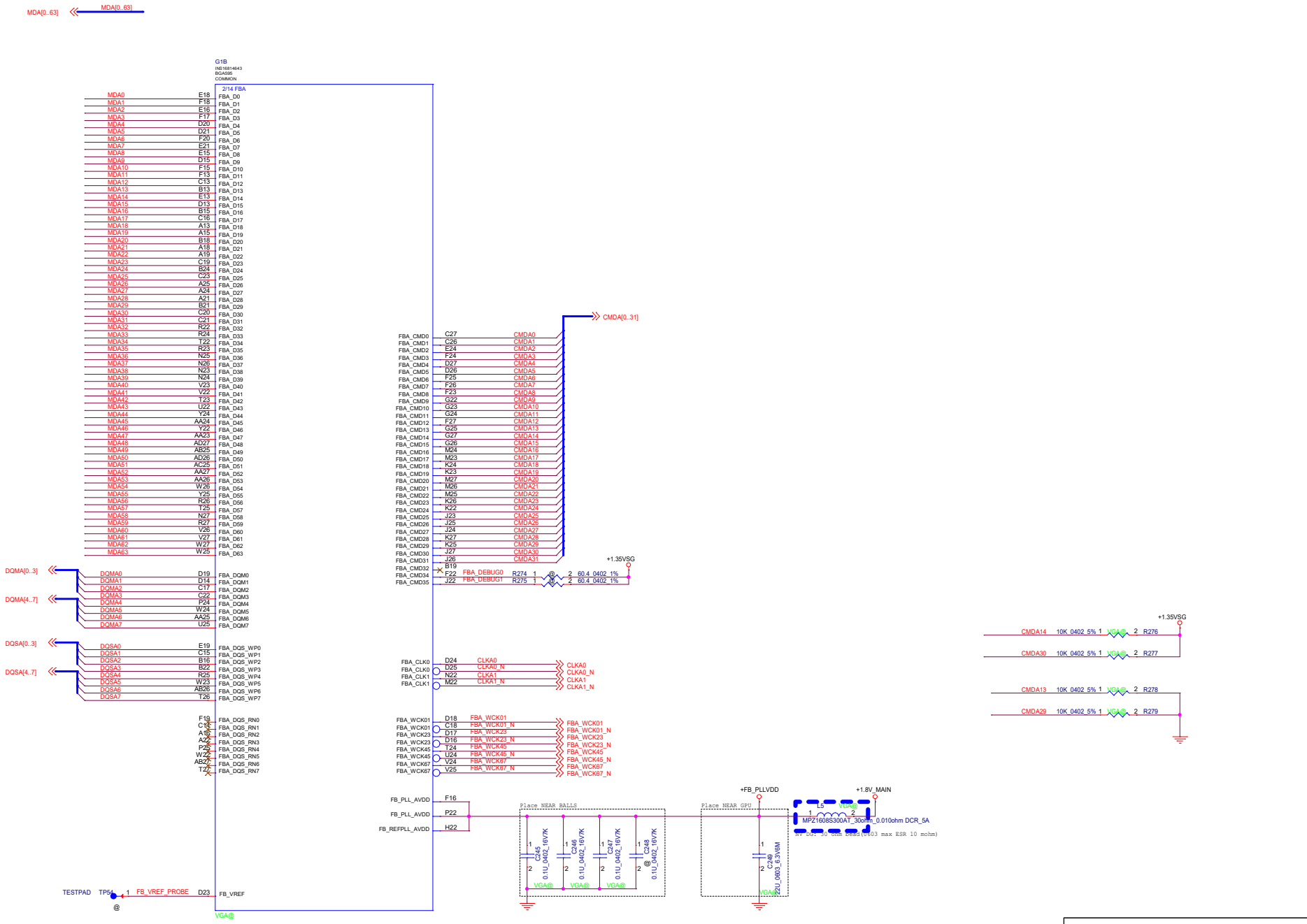

FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)
FBB_PLL_AVDD	1		1 X 30Ω bead (0603 max ESR 10 mΩ)
FB_REFPLL_AVDD	1	1.8V	0.1uF (0402 X5R)
			1 X 22uF (0805)

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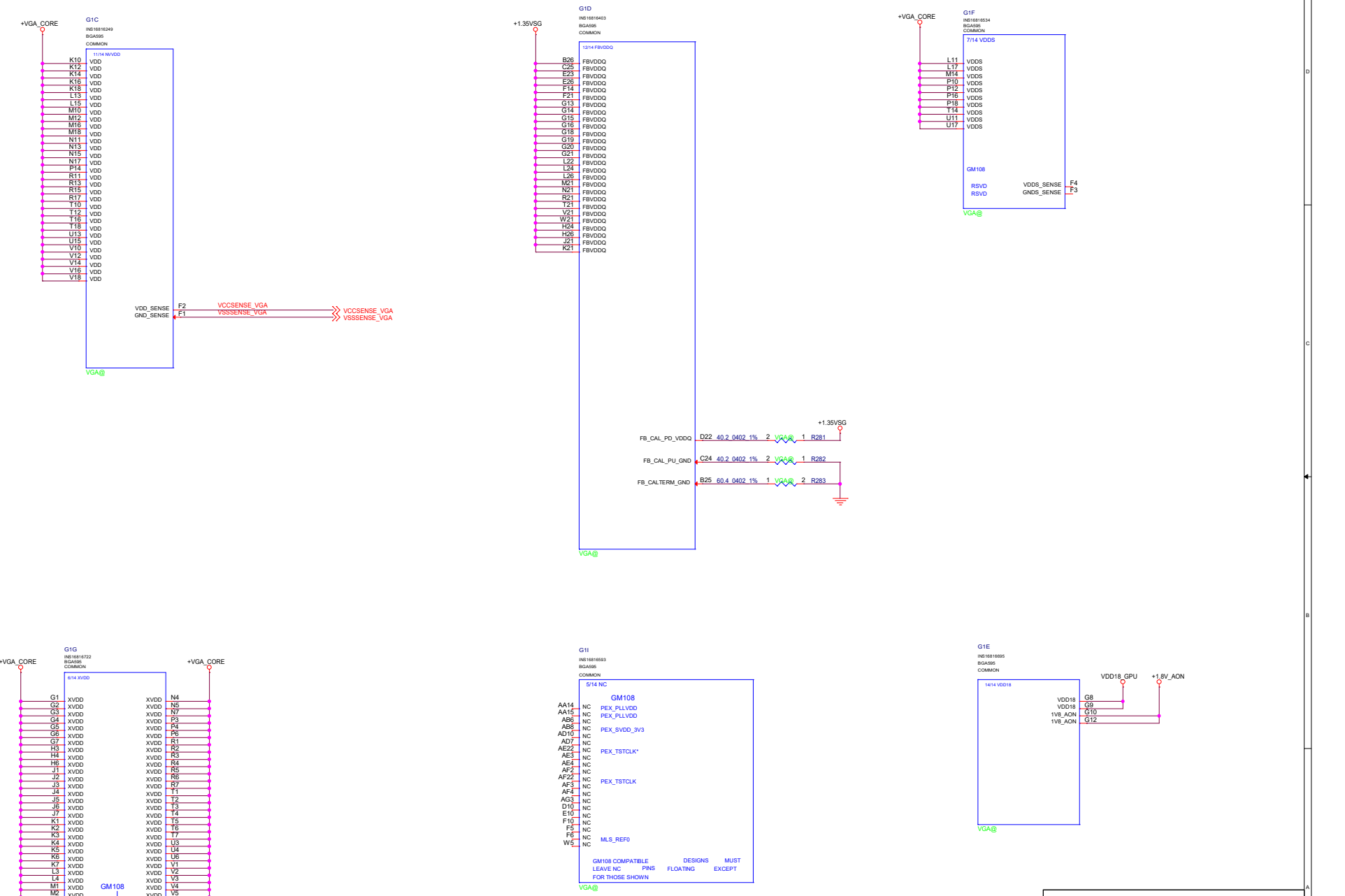

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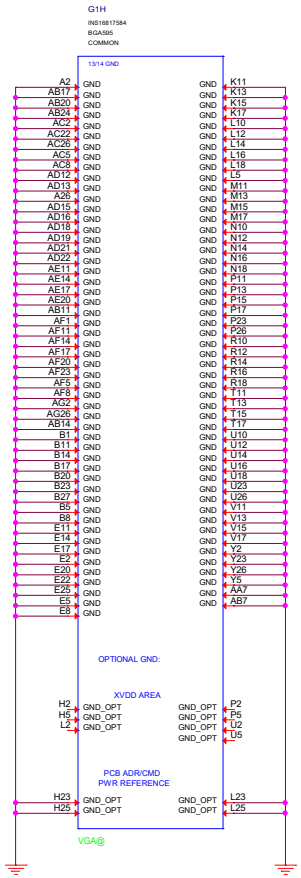

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Title
GPU GND

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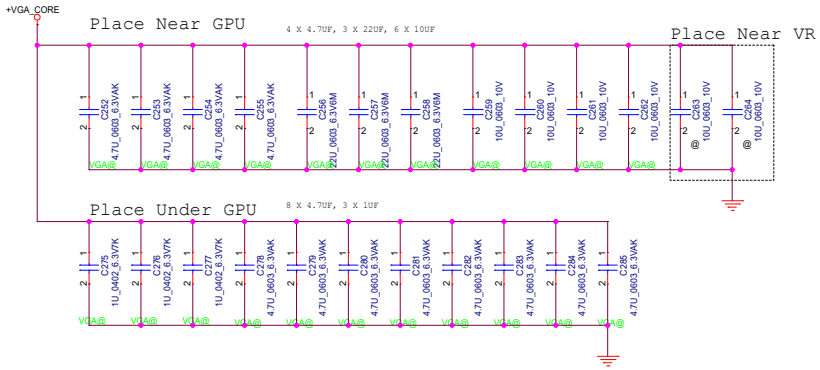

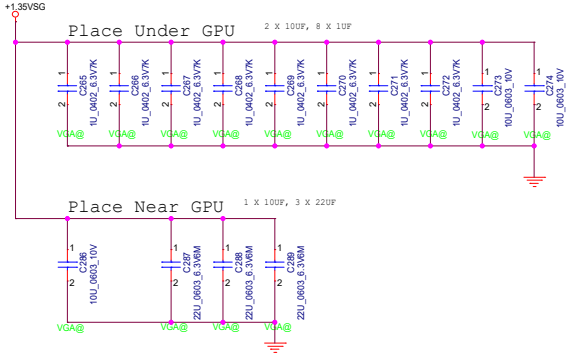

Table 7.18 GB2C-64 Package: Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
NVVDD	31	Varies	3 X 1uF (0402) 8 X 4.7uF (0603)	4 X 4.7uF (0805) 4 X 10uF (0805) 3 X 22uF (0805) 1 X 330uF (Poscap) Near VR: 2 X 10uF (0805)
NVVDDS	10	Varies	2 X 1uF (0402) 4 X 4.7uF (0603)	7 X 10uF (0805) 1 X 22uF (0805) 1 X 330uF (Poscap)
FBVDDQ (GPU side)[1]	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)

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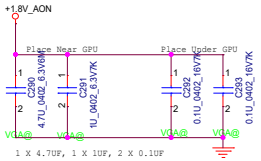
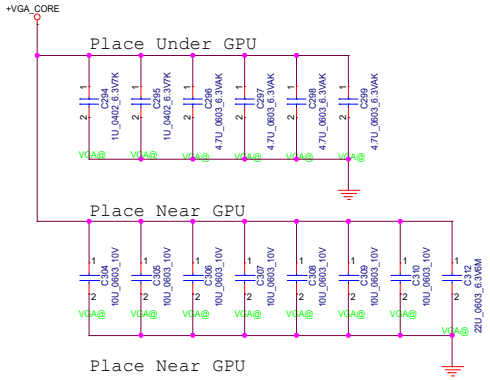
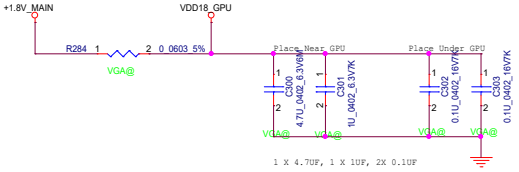




1 x 22uF
7x 10uF
4 x 4.7uF
2 x 1uF



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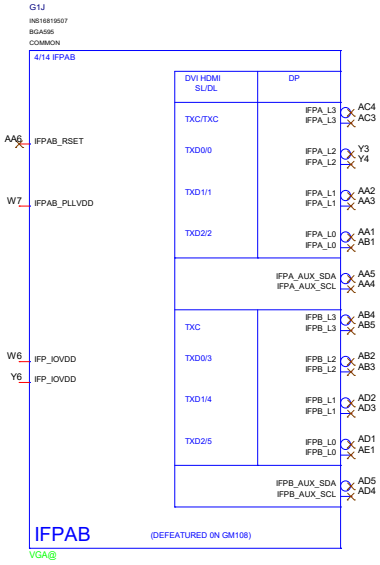

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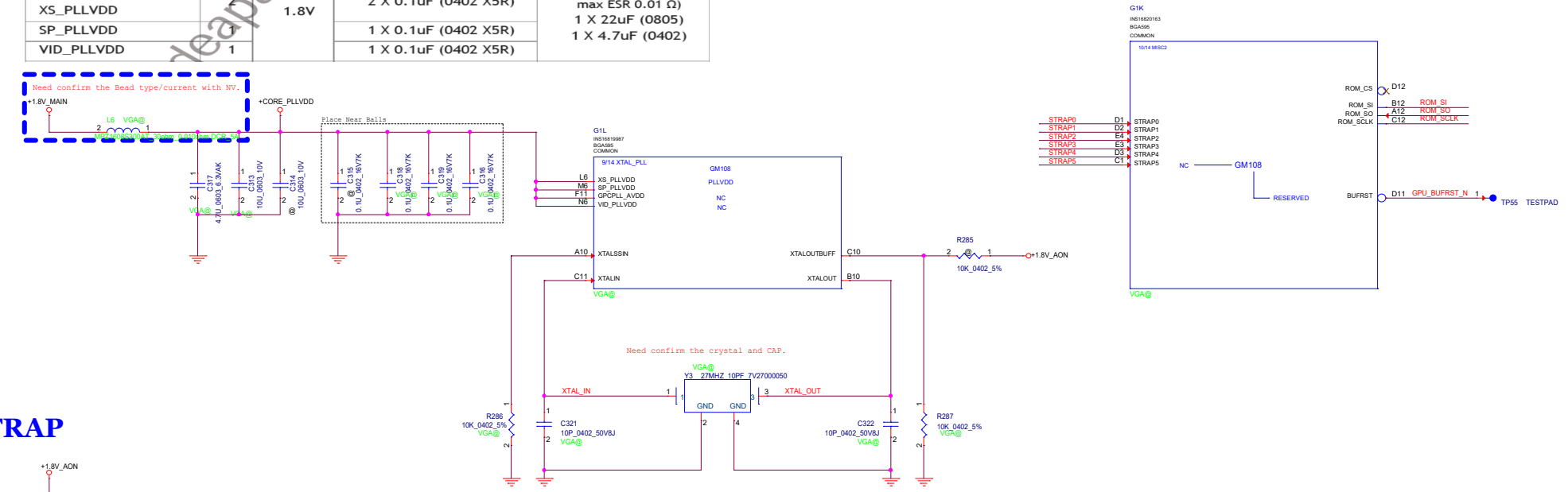
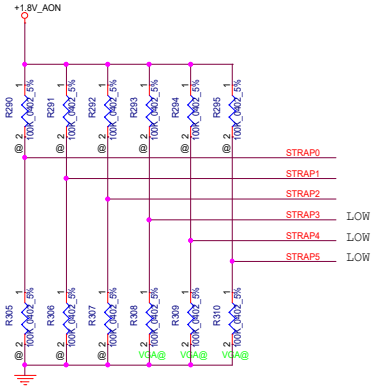
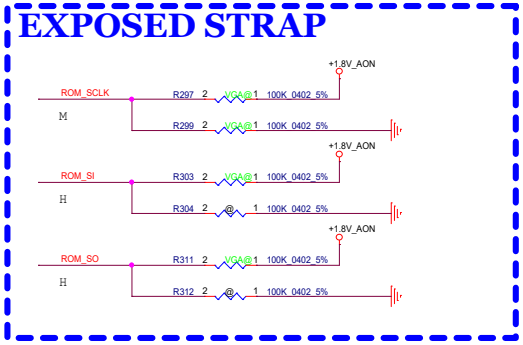
GPCPLL_AVDDx	2	1.8V	2 X 0.1uF (0402 X5R)	1 X 30Ω bead (0603 max ESR 0.01 Ω) 1 X 22uF (0805) 1 X 4.7uF (0402)
XS_PLLVDD				
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	
VID_PLLVDD	1		1 X 0.1uF (0402 X5R)	



STRAP



EXPOSED STRAP



STRAP0~2 , Please ref RVL for BOM stuffing
Micron: L M L
Hynix : H M L

GDDR5 RAM_CFG															
GPU SKU	GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memroy configuration	Vendor	Manufacturer Part Nurnber	Die Revision	Memory Speed CK Grad	Memory D/C Minimum	Strap	Strap2	Strap1	Strap0	Status
	N17S-G1	GDDR5	1.35V	8Gb	256Mx32	Samsung	K4G80325FB-HC28	B-die	7 Gbps	N/A	0x0	L	L	L	Prodution ready
							K4G80325FB-HC25		8 Gbps	N/A					Substitution allowed with waiver
						Micron	MT51J256M32HF-70:A	A-die	7 Gbps	N/A	0x1	L	L	H	Prodution ready
							MT51J256M32HF-80:A		8 Gbps	N/A					Substitution allowed with waiver
						Hynix	H5GC8H24MJR-R0C	M-die	7 Gbps	N/A	0x2	L	H	L	Post-Prodution Candidate
							H5GC8H24MJR-R4C		8 Gbps	N/A					Substitution allowed with waiver
						Micron	MT51J256M32HF-70:B	B-die	7 Gbps	N/A	0x4	H	L	L	Post-Prodution ready
							MT51J256M32HF-80:B		8 Gbps	N/A					Substitution allowed with waiver
						Hynix	H5GC8H24AJR-R0C	A-die	7 Gbps	N/A	0x5	H	L	H	Post-Prodution ready
							H5GC8H24AJR-R2C		8 Gbps	N/A					Substitution allowed with waiver

GDDR5 RAM_CFG															
GPU SKU	GPU	Memory Type	FBVDD/ FBVDDQ	Memory Density	Memroy configuration	Vendor	Manufacturer Part Nurnber	Die Revision	Memory Speed CK Grad	Memory D/C Minimum	Strap	Strap2	Strap1	Strap0	Status
	N17S-G0/G2	GDDR5	1.35V	8Gb	256Mx32	Micron	MT51J256M32HF-80:B	B-die	8 Gbps	N/A	0x9	L	M	L	Prodution ready
					512Mx16	Hynix	H5GC8H24AJR-R2C	A-die	8 Gbps	N/A	0xA	L	M	H	Prodution ready

ROM_SCLK(LSB)/ROM_SI/ROM_SO(MSB) : H H M

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins (see Note)			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	disabled	ENABLED	ENABLED
12	L	H	H	ENABLED	disabled	ENABLED	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	L	ENABLED	disabled	disabled	disabled
9	H	H	H	disabled	disabled	disabled	disabled
	All other Strap Configurations			(Reserved, do not configure)			
				(Reserved)			

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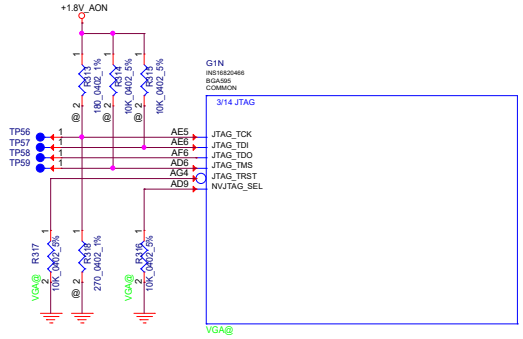

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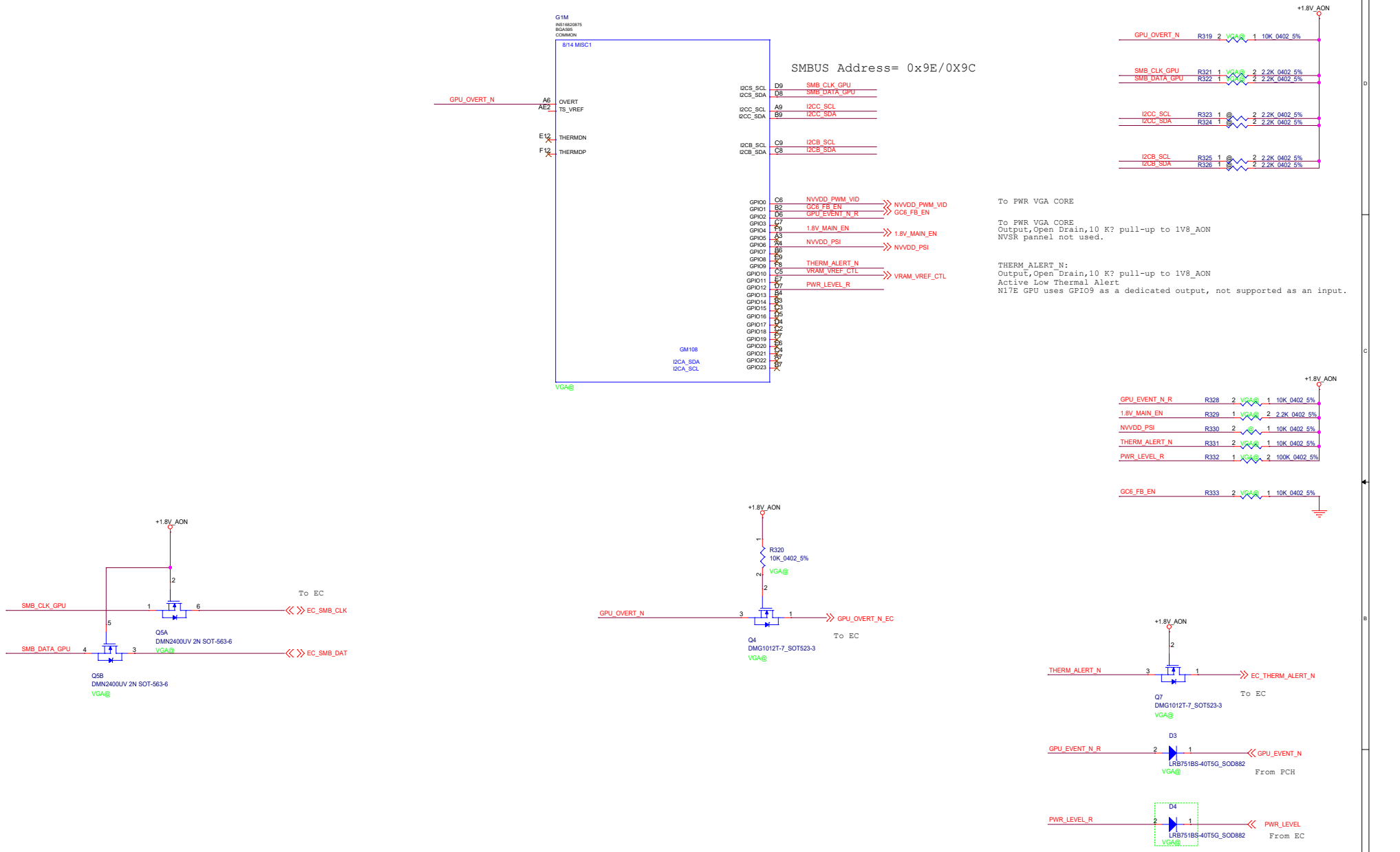
G1M
INS16820875
BGA595
COMMON
8/14 MISC1
SMBUS Address= 0x9E/0X9C
GPU_OVERT_N
OVERT
TS_VREF
THERMDN
THERMDP
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
SMB_CLK_GPU
SMB_DATA_GPU
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
NVVDD_PWM_VID
GC6_FB_EN
GPU_EVENT_N_R
1.8V_MAIN_EN
NVVDD_PSI
THERM_ALERT_N
VRAM_VREF_CTL
PWR_LEVEL_R
GM108
I2CA_SDA
I2CA_SCL
VGA@
+1.8V_AON
GPU_OVERT_N R319 2 VGA@ 1 10K_0402_5%
SMB_CLK_GPU R321 1 VGA@ 2 2.2K_0402_5%
SMB_DATA_GPU R322 1 VGA@ 2 2.2K_0402_5%
I2CC_SCL R323 1 @ 2 2.2K_0402_5%
I2CC_SDA R324 1 @ 2 2.2K_0402_5%
I2CB_SCL R325 1 @ 2 2.2K_0402_5%
I2CB_SDA R326 1 @ 2 2.2K_0402_5%
To PWR VGA CORE
To PWR VGA CORE
Output,Open Drain,10 K? pull-up to 1V8_AON
NVSR pannel not used.
THERM_ALERT_N:
Output,Open Drain,10 K? pull-up to 1V8_AON
Active Low Thermal Alert
N17E GPU uses GPIO9 as a dedicated output, not supported as an input.
+1.8V_AON
GPU_EVENT_N_R R328 2 VGA@ 1 10K_0402_5%
1.8V_MAIN_EN R329 1 VGA@ 2 2.2K_0402_5%
NVVDD_PSI R330 2 @ 1 10K_0402_5%
THERM_ALERT_N R331 2 VGA@ 1 10K_0402_5%
PWR_LEVEL_R R332 1 VGA@ 2 100K_0402_5%
GC6_FB_EN R333 2 VGA@ 1 10K_0402_5%
+1.8V_AON
SMB_CLK_GPU
SMB_DATA_GPU
Q5A
DMN2400UV 2N SOT-563-6
VGA@
Q5B
DMN2400UV 2N SOT-563-6
VGA@
To EC
EC_SMB_CLK
EC_SMB_DAT
+1.8V_AON
R320
10K_0402_5%
VGA@
GPU_OVERT_N
Q4
DMG1012T-7_SOT523-3
VGA@
To EC
GPU_OVERT_N_EC
+1.8V_AON
THERM_ALERT_N
Q7
DMG1012T-7_SOT523-3
VGA@
To EC
EC_THERM_ALERT_N
D3
GPU_EVENT_N_R
LRB751BS-40T5G_SOD882
VGA@
From PCH
GPU_EVENT_N
D4
PWR_LEVEL_R
LRB751BS-40T5G_SOD882
VGA@
From EC
PWR_LEVEL
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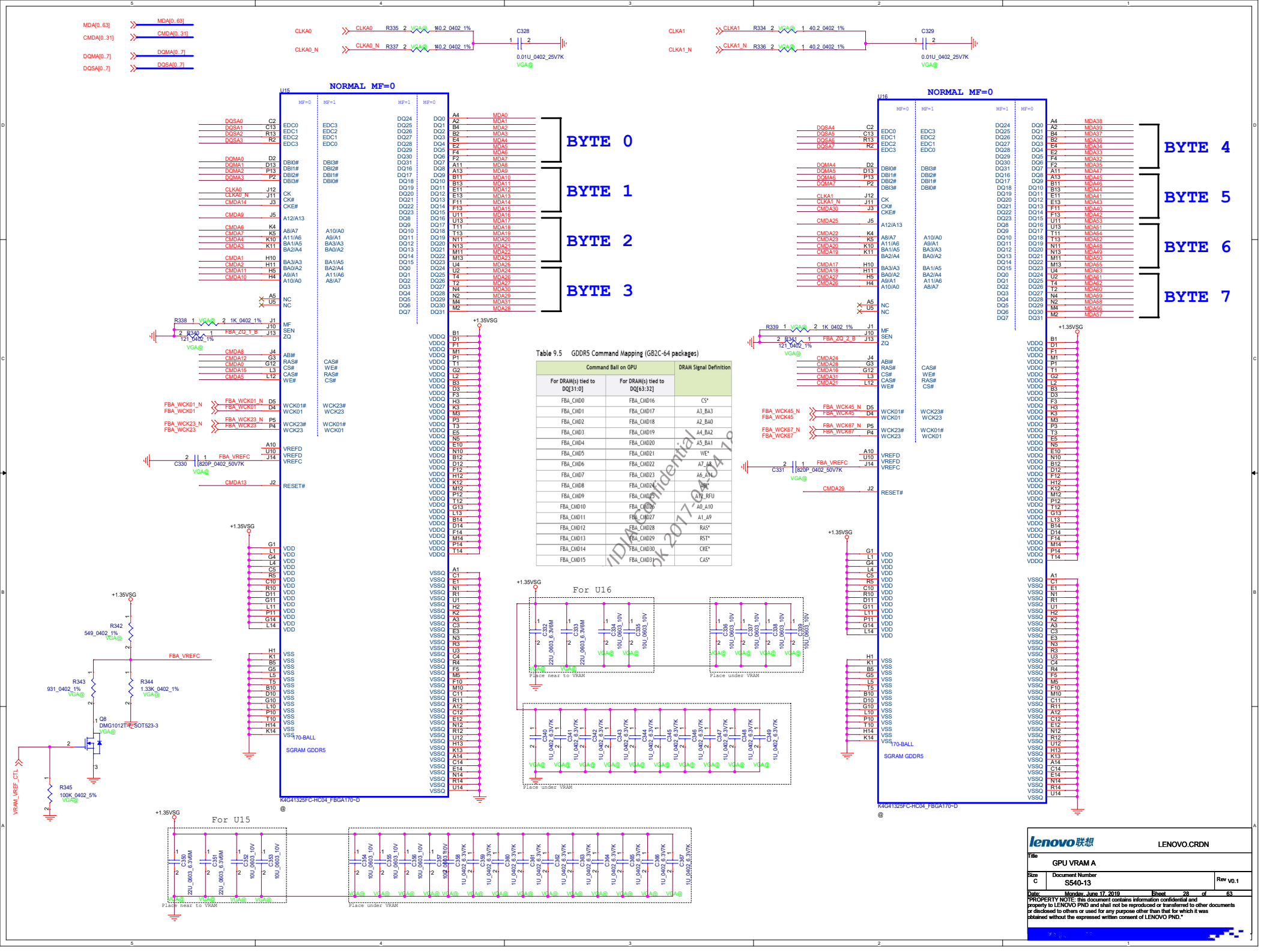

Table 9.5 GDDR5 Command Mapping (GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	CAS*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CA5*

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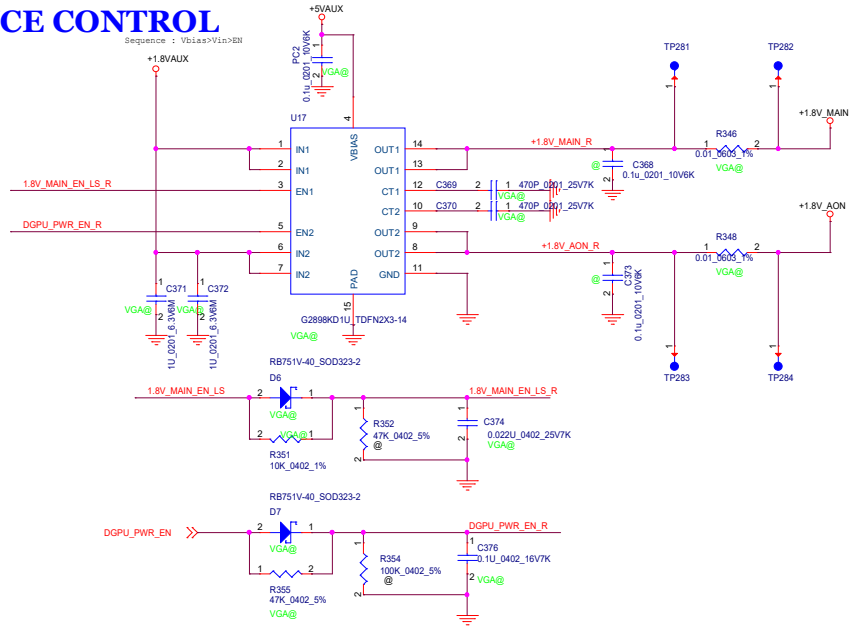
POWER SEQUENCE CONTROL



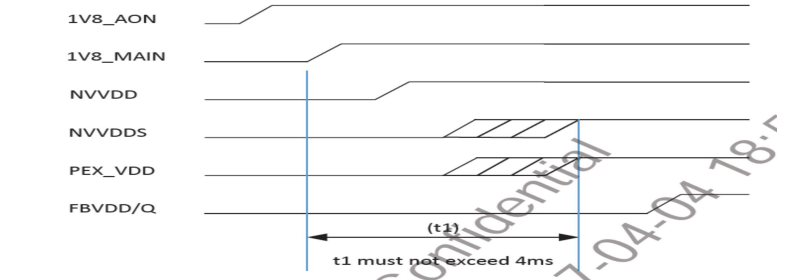


Figure 7.5 Example of Power-Up Sequencing Order

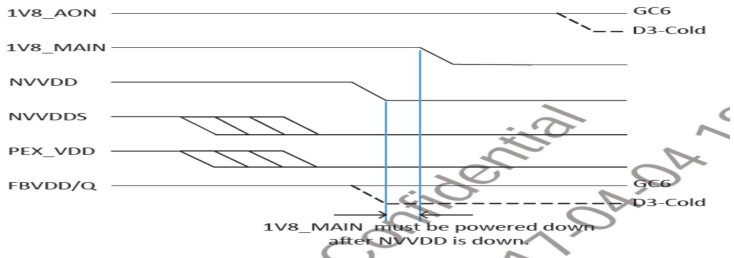
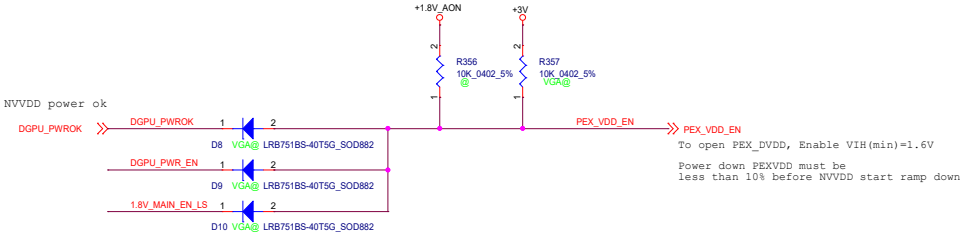
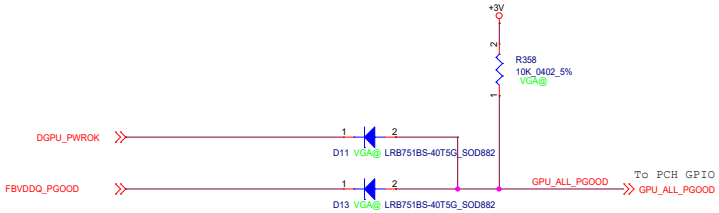
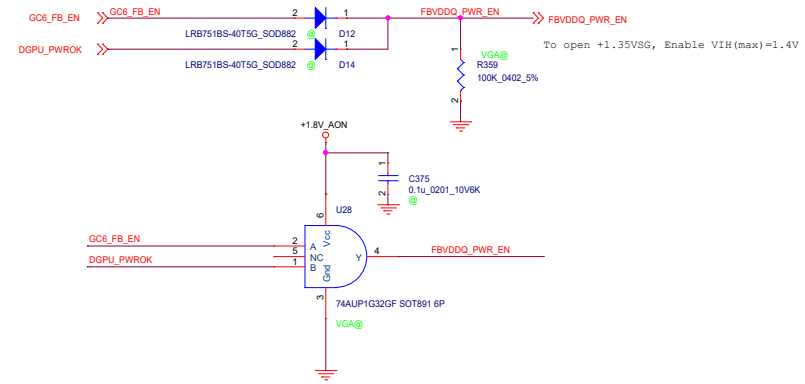
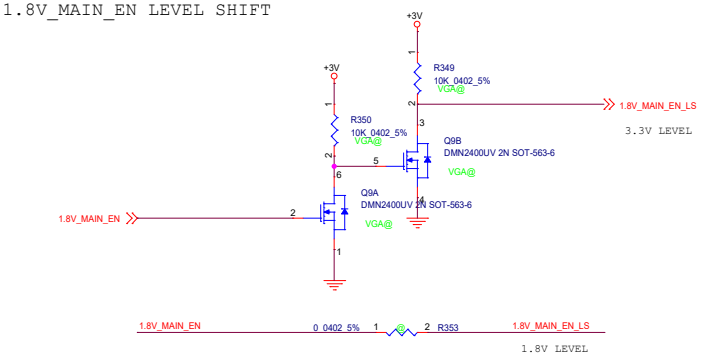


Figure 7.6 Example of Power-Down Sequencing Order









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Title: GPU Switch/Thermal		
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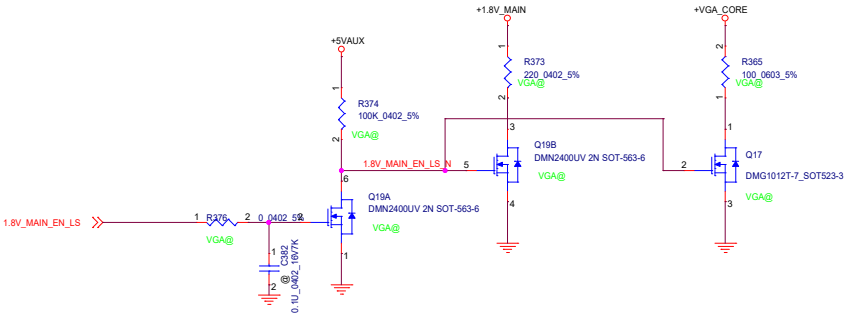

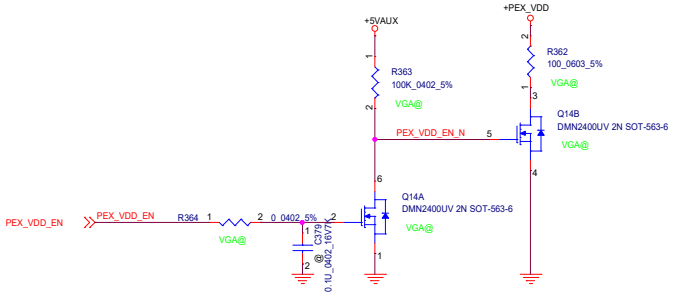

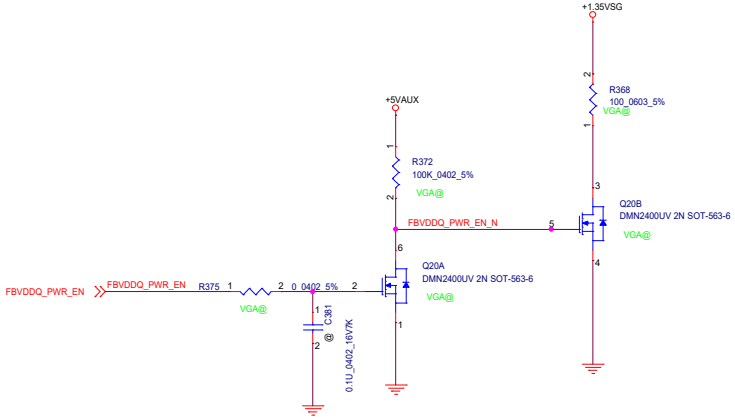

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Title: GPU POWER DISCHARGE

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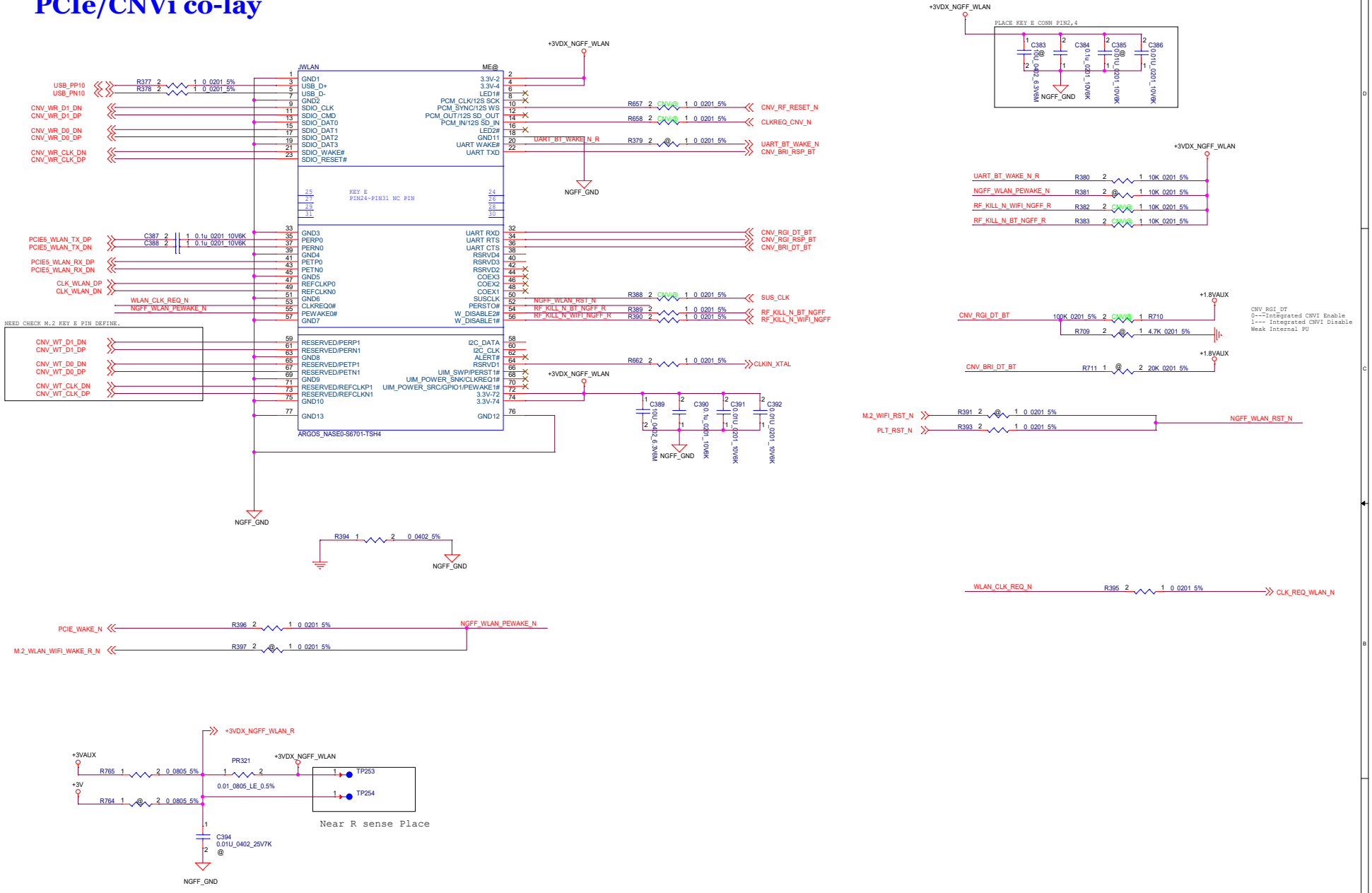
PCIe/CNVi co-lay



lenovo联想		LENOVO.CRDN	
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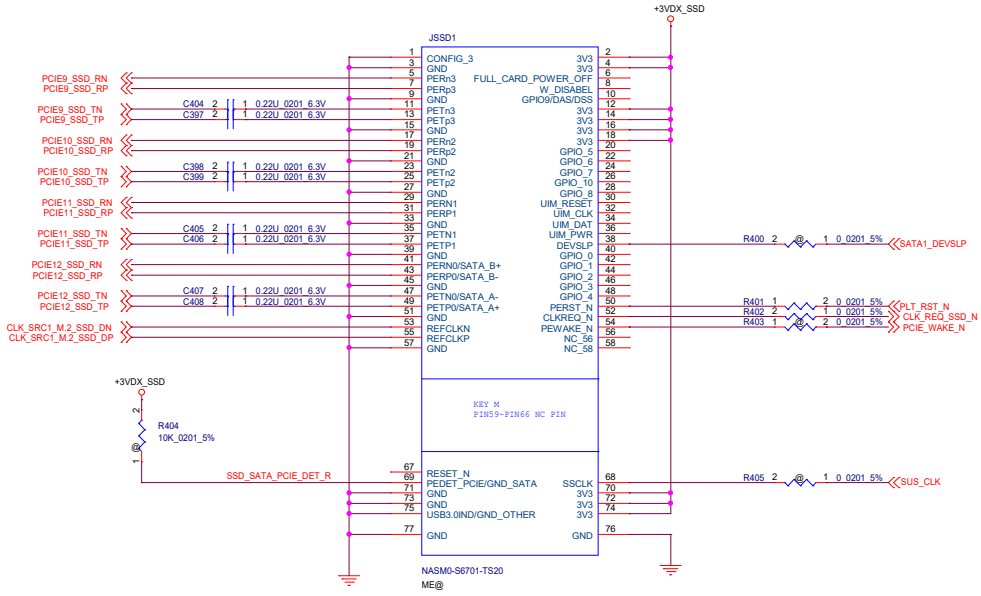

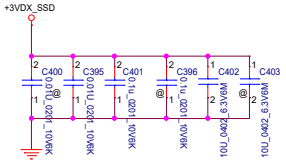

lenovo联想	LENOVO.CRDN	
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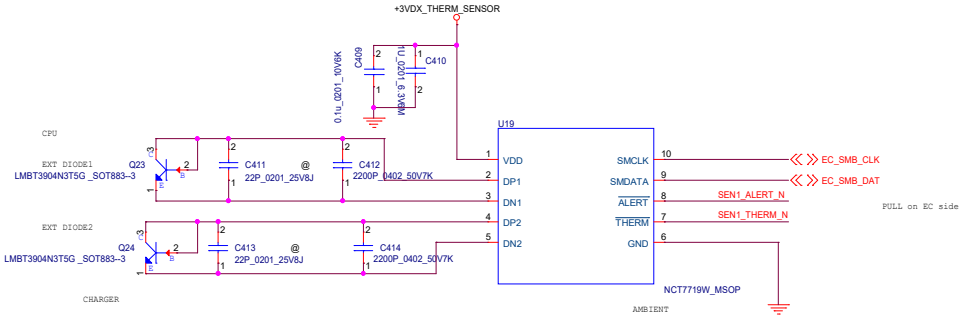

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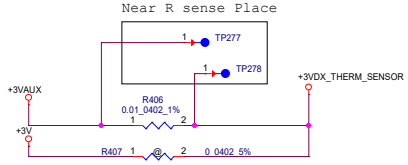

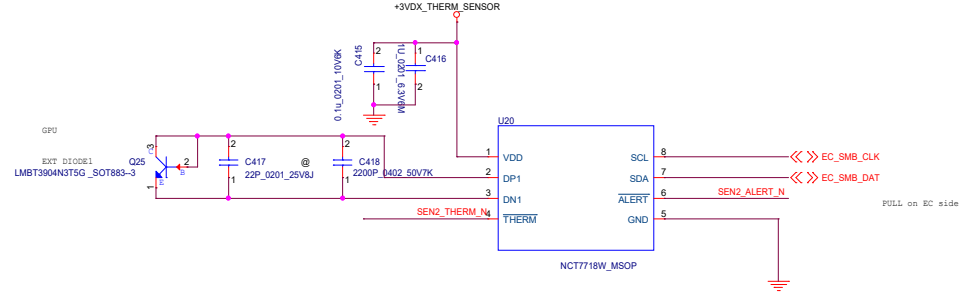

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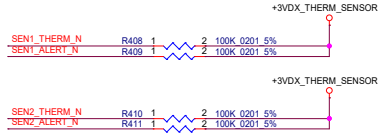

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Title: ThermalSensor

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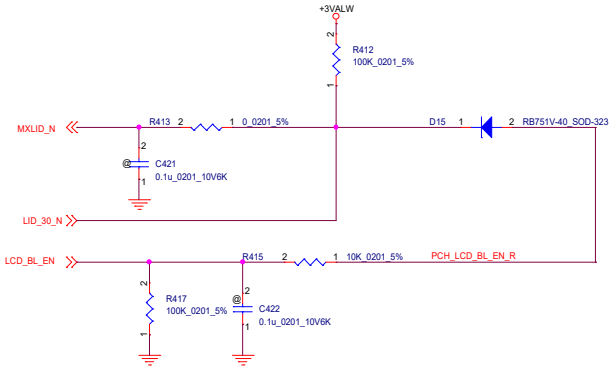

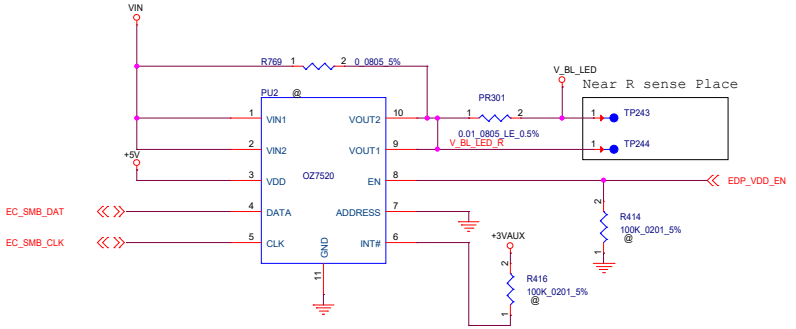

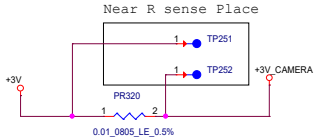

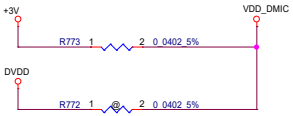

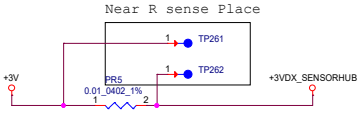

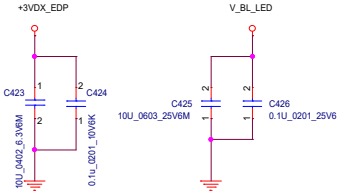

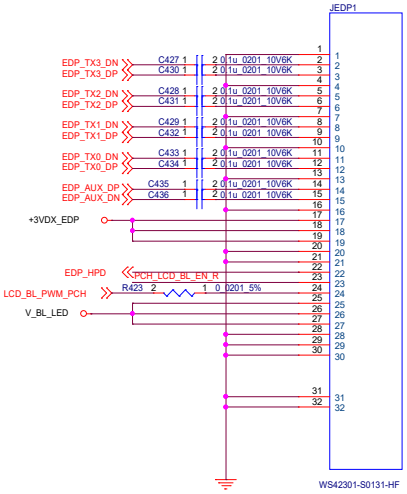

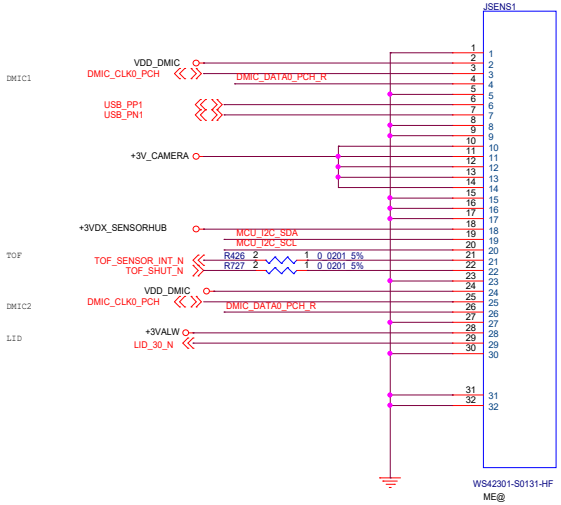

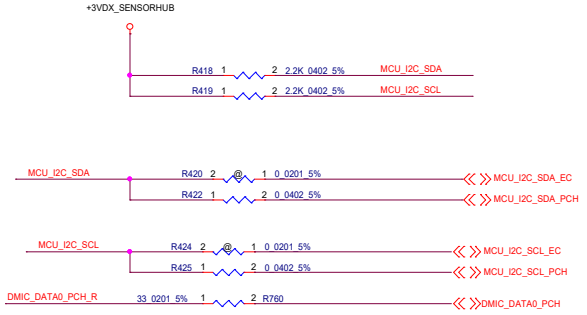

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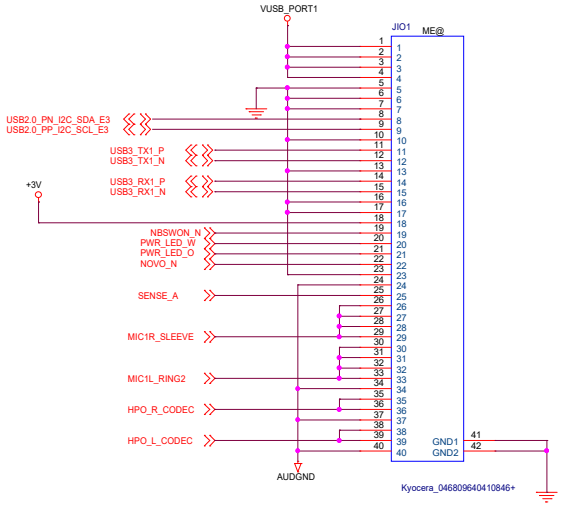

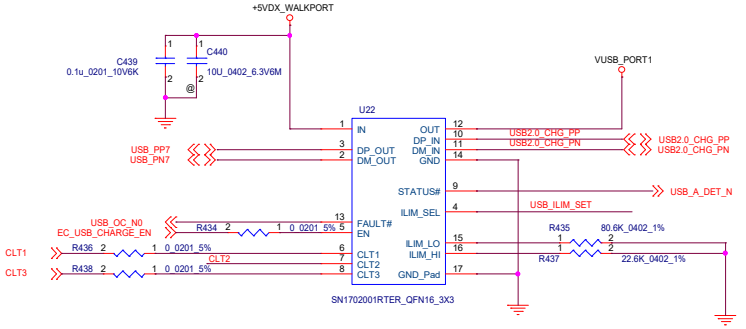

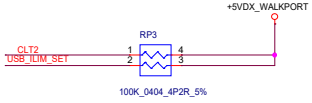


```
Install ILIM_SEL shunt for ILIM = ILIM_LO = 0.63A
Remove ILIM_SEL shunt for ILIM =ILIM_HI = 2.3A
Support Mouse/Keyboard wake up.
Support Power Wake
CLT1      CLT3
 1         0   --    SDP
 0         1   --    DCP/Auto
```

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Title: USB 3.1 GEN2

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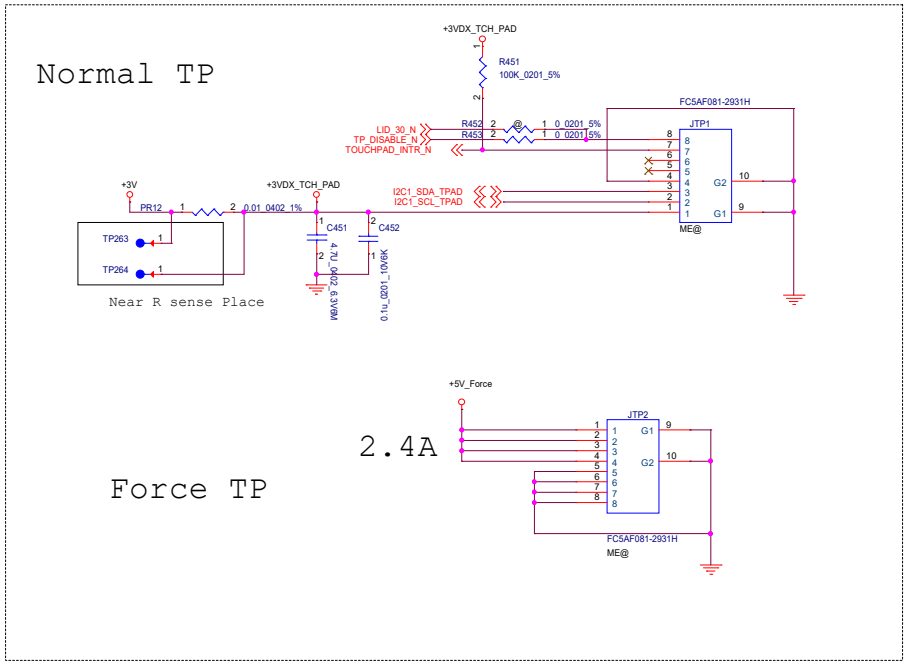

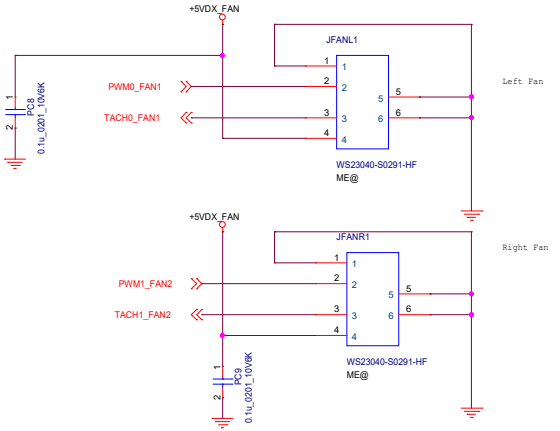

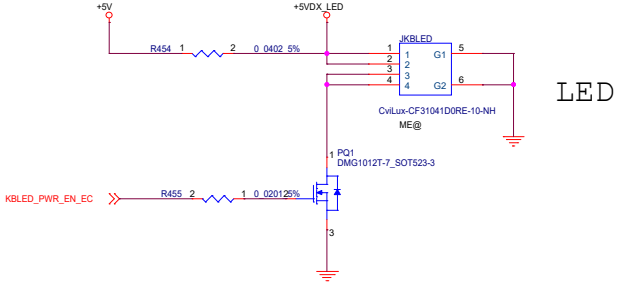

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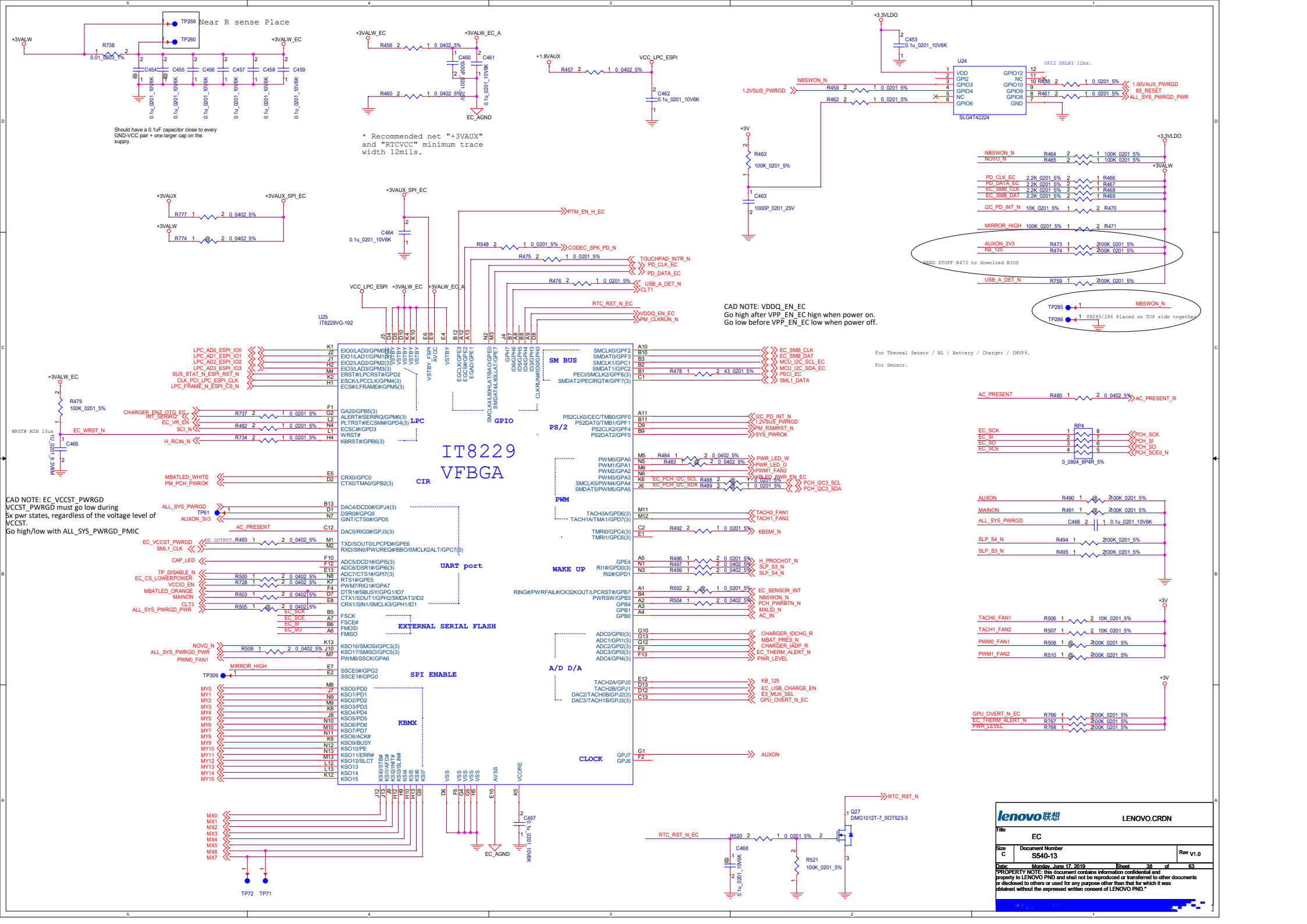
Near R sense Place
TP259
TP260
R738
0.01_0603_1%
+3VALW
+3VALW_EC
C454
C455
C456
C457
C458
C459
0.1u_0201_10V6K
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.
+3VALW_EC
+3VALW_EC_A
R456
R460
C460
C461
0.1u_0201_10V6K
EC_AGND
* Recommended net "+3VAUX" and "RTCVCC" minimum trace width 12mils.
+1.8VAUX
VCC_LPC_ESPI
R457
C462
0.1u_0201_10V6K
+3.3VLDO
C453
0.1u_0201_10V6K
U24
GPI2 DELAY 12ms.
VDD
GPI2
GPIO3
GPIO4
NC
GPIO6
GPIO12
NC
GPIO10
GPIO9
GPIO8
GND
SLG4T42224
NBSWON_N
1.2VSUS_PWRGD
R459
R462
R458
R461
1.00VAUX_PWRGD
8S_RESET
ALL_SYS_PWRGD_PWR
+3V
R463
100K_0201_5%
C463
1000P_0201_25V
+3.3VLDO
+3VALW
NBSWON_N
NOVO_N
R464
R465
100K_0201_5%
PD_CLK_EC
PD_DATA_EC
EC_SMB_CLK
EC_SMB_DAT
2.2K_0201_5%
R466
R467
R468
R469
I2C_PD_INT_N
10K_0201_5%
R470
MIRROR_HIGH
100K_0201_5%
R471
AUXON_3V3
KB_125
R473
R474
200K_0201_5%
NEED STUFF R473 to download BIOS
USB_A_DET_N
R759
TP285
TP286
NBSWON_N
TP285/286 Placed on TOP side together
+3VAUX
+3VAUX_SPI_EC
R777
+3VALW
R774
+3VAUX_SPI_EC
C464
0.1u_0201_10V6K
PTM_EN_H_EC
R548
CODEC_SPK_PD_N
R475
TOUCHPAD_INTR_N
PD_CLK_EC
PD_DATA_EC
R476
USB_A_DET_N
CLT1
RTC_RST_N_EC
VDDQ_EN_EC
PM_CLKRUN_N
VCC_LPC_ESPI
+3VALW_EC
+3VALW_EC_A
U25
IT8229VG-192
CAD NOTE: VDDQ_EN_EC
Go high after VPP_EN_EC hign when power on.
Go low before VPP_EN_EC low when power off.
IT8229
VFBGA
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
KBMX
CLOCK
LPC_AD0_ESPI_IO0
LPC_AD1_ESPI_IO1
LPC_AD2_ESPI_IO2
LPC_AD3_ESPI_IO3
SUS_STAT_N_ESPI_RST_N
CLK_PCI_LPC_ESPI_CLK
LPC_FRAME_N_ESPI_CS_N
SMCLK0/GPF2
SMDAT0/GPF3
SMCLK1/GPC1
SMDAT1/GPC2
PECI/SMCLK2/GPF6(3)
SMDAT2/PECIRQT#/GPF7(3)
EC_SMB_CLK
EC_SMB_DAT
MCU_I2C_SCL_EC
MCU_I2C_SDA_EC
PECI_EC
SML1_DATA
R478
2_43_0201_5%
+3VALW_EC
R479
100K_0201_5%
WRST# MIN 10us
EC_WRST_N
C465
0.1u_0201_10V6K
CHARGER_ENZ_OTG_EC
INT_SERIRQ
EC_VR_ON
SCI_N
H_RCIN_N
R737
R482
R734
GA20/GPB5(3)
ALERT#/SERIRQ/GPM6(3)
PLTRST#/ECSMI#/GPD4(3)
ECSCI#/GPD3
WRST#
KBRST#/GPB6(3)
PS2CLK0/CEC/TMB0/GPF0
PS2DAT0/TMB1/GPF1
PS2CLK2/GPF4
PS2DAT2/GPF5
I2C_PD_INT_N
1.2VSUS_PWRGD
PM_RSMRST_N
SYS_PWROK
MBATLED_WHITE
PM_PCH_PWROK
CRX0/GPC0
CTX0/TMA0/GPB2(3)
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
SMCLK5/PWM4/GPA4
SMDAT5/PWM5/GPA5
PWR_LED_W
PWR_LED_O
PWM1_FAN2
KBLED_PWR_EN_EC
EC_PCH_I2C_SCL
EC_PCH_I2C_SDA
PCH_I2C3_SCL
PCH_I2C3_SDA
R484
R483
R488
R489
TACH0A/GPD6(3)
TACH1A/TMA1/GPD7(3)
TACH0_FAN1
TACH1_FAN2
TMRI0/GPC4(3)
TMRI1/GPC6(3)
KBSMI_N
R492
ALL_SYS_PWRGD
TP61
AUXON_3V3
AC_PRESENT
DAC4/DCD0#/GPJ4(3)
DSR0#/GPG6
CINT/CTS0#/GPD5
DAC5/RIG0#/GPJ5(3)
EC_VCCST_PWRGD
SML1_CLK
OD_OUTPUT.R493
TXD/SOUT0/LPCPD#/GPE6
RXD/SIN0/PWUREQ#/BBO/SMCLK2ALT/GPC7(3)
CAP_LED
ADC5/DCD1#/GPI5(3)
ADC6/DSR1#/GPI6(3)
ADC7/CTS1#/GPI7(3)
RTS1#/GPE5
PWM7/RIG1#/GPA7
DTR1#/SBUSY/GPG1/ID7
CTX1/SOUT1/GPH2/SMDAT3/ID2
CRX1/SIN1/SMCLK3/GPH1/ID1
TP_DISABLE_N
EC_CS_LOWERPOWER
VCCIO_EN
MBATLED_ORANGE
MAINON
CLT3
ALL_SYS_PWRGD_PWR
R500
R728
R503
R505
EC_SCK
EC_SCE
EC_SI
EC_SO
FSCK
FSCE#
FMOSI
FMISO
NOVO_N
ALL_SYS_PWRGD_PWR
PWM0_FAN1
R509
KSO16/SMOSI/GPC3(3)
KSO17/SMISO/GPC5(3)
PWM6/SSCK/GPA6
MIRROR_HIGH
TP309
SSCE0#/GPG2
SSCE1#/GPG0
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
MY8
MY9
MY10
MY11
MY12
MY13
MY14
MY15
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
TP72
TP71
EC_AGND
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7
PWRSW/GPB3
GPB4
GPB1
GPB0
EC_SENSOR_INT
NBSWON_N
PCH_PWRBTN_N
MXLID_N
AC_IN
R502
R504
ADC0/GPI0(3)
ADC1/GPI1(3)
ADC2/GPI2(3)
ADC3/GPI3(3)
ADC4/GPI4(3)
CHARGER_IDCHG_R
MBAT_PRES_N
CHARGER_IADP_R
EC_THERM_ALERT_N
PWR_LEVEL
TACH2A/GPJ0
TACH2B/GPJ1
DAC2/TACH0B/GPJ2(3)
DAC3/TACH1B/GPJ3(3)
KB_125
EC_USB_CHARGE_EN
E3_MUX_SEL
GPU_OVERT_N_EC
GPJ7
GPJ6
AUXON
RTC_RST_N
RTC_RST_N_EC
R520
C468
R521
Q27
DMG1012T-7_SOT523-3
C467
0.1u_0201_10V6K
For Thermal Sensor / BL / Battery / Charger / IMVP9.
For Sensor.
AC_PRESENT
R480
AC_PRESENT_R
EC_SCK
EC_SI
EC_SO
EC_SCE
RP4
PCH_SCK
PCH_SI
PCH_SO
PCH_SCE0_N
0_0804_8P4R_5%
AUXON
MAINON
ALL_SYS_PWRGD
SLP_S4_N
SLP_S3_N
R490
R491
R494
R495
TACH0_FAN1
TACH1_FAN2
PWM0_FAN1
PWM1_FAN2
R506
R507
R508
R510
10K_0201_5%
GPU_OVERT_N_EC
EC_THERM_ALERT_N
PWR_LEVEL
R766
R767
R768
CAD NOTE: EC_VCCST_PWRGD
VCCST_PWRGD must go low during
Sx pwr states, regardless of the voltage level of
VCCST.
Go high/low with ALL_SYS_PWRGD_PMIC
lenovo联想
LENOVO.CRDN
Title
EC
Size
C
Document Number
S540-13
Rev V1.0
Date: Monday, June 17, 2019
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Title: BLANK

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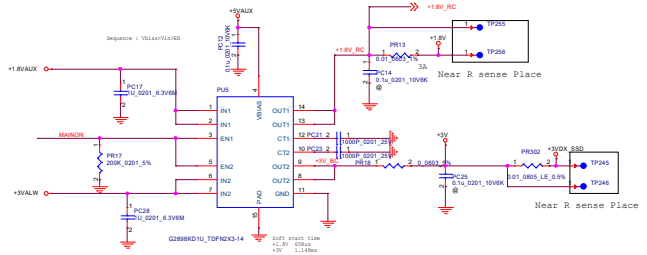

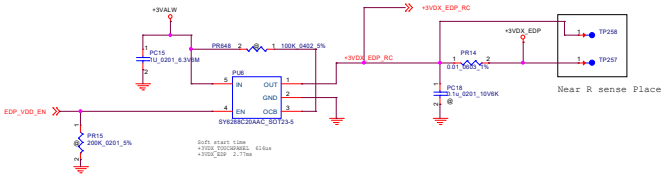

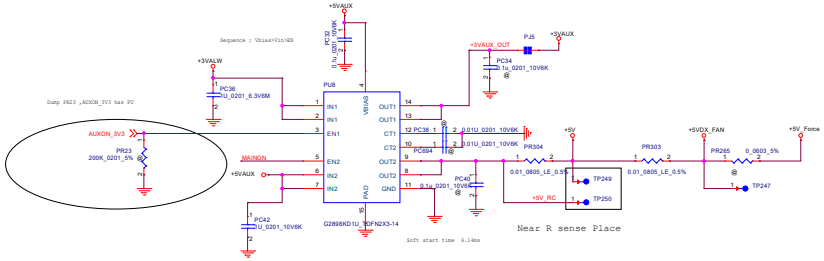

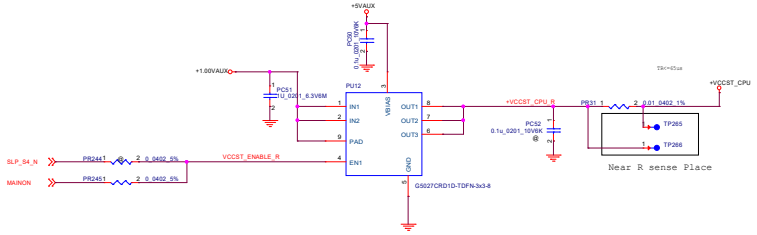

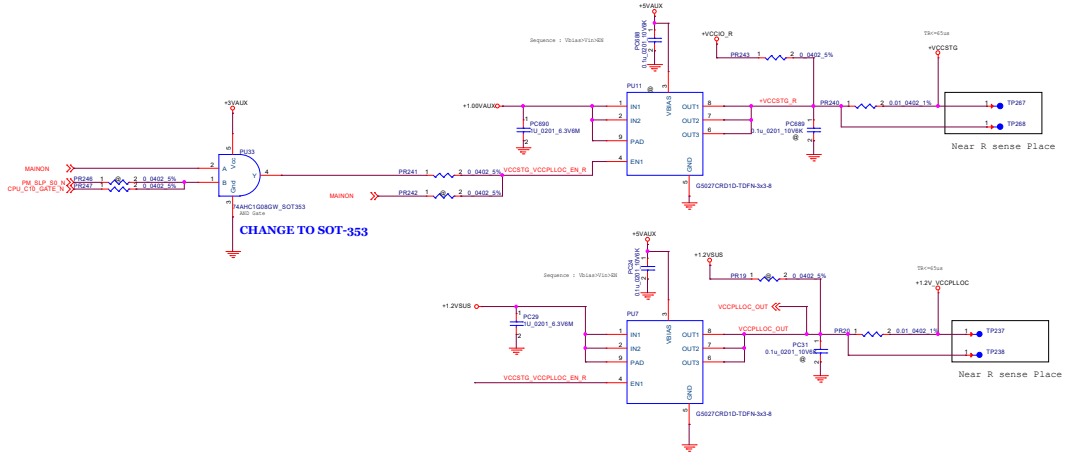

lenovo 联想	LENOVO.CRDN	
Title: SWITCH POWER		
Size: D	Document Number: S540-13	Rev V1.0
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Title: BLANK

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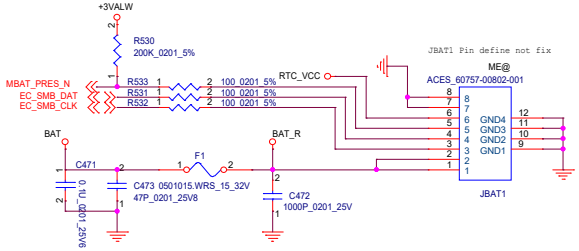

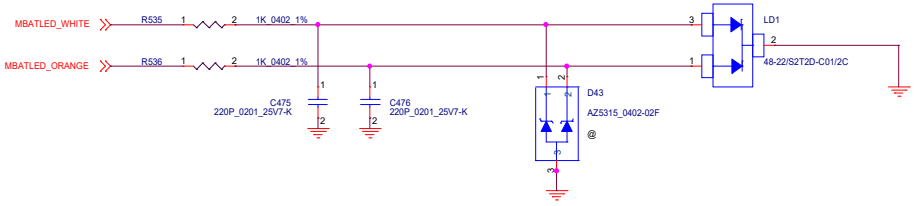

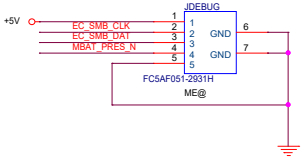

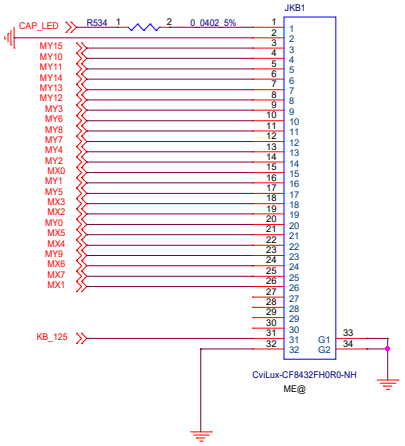

lenovo联想 LENOVO.CRDN

Title: CONNECTOR

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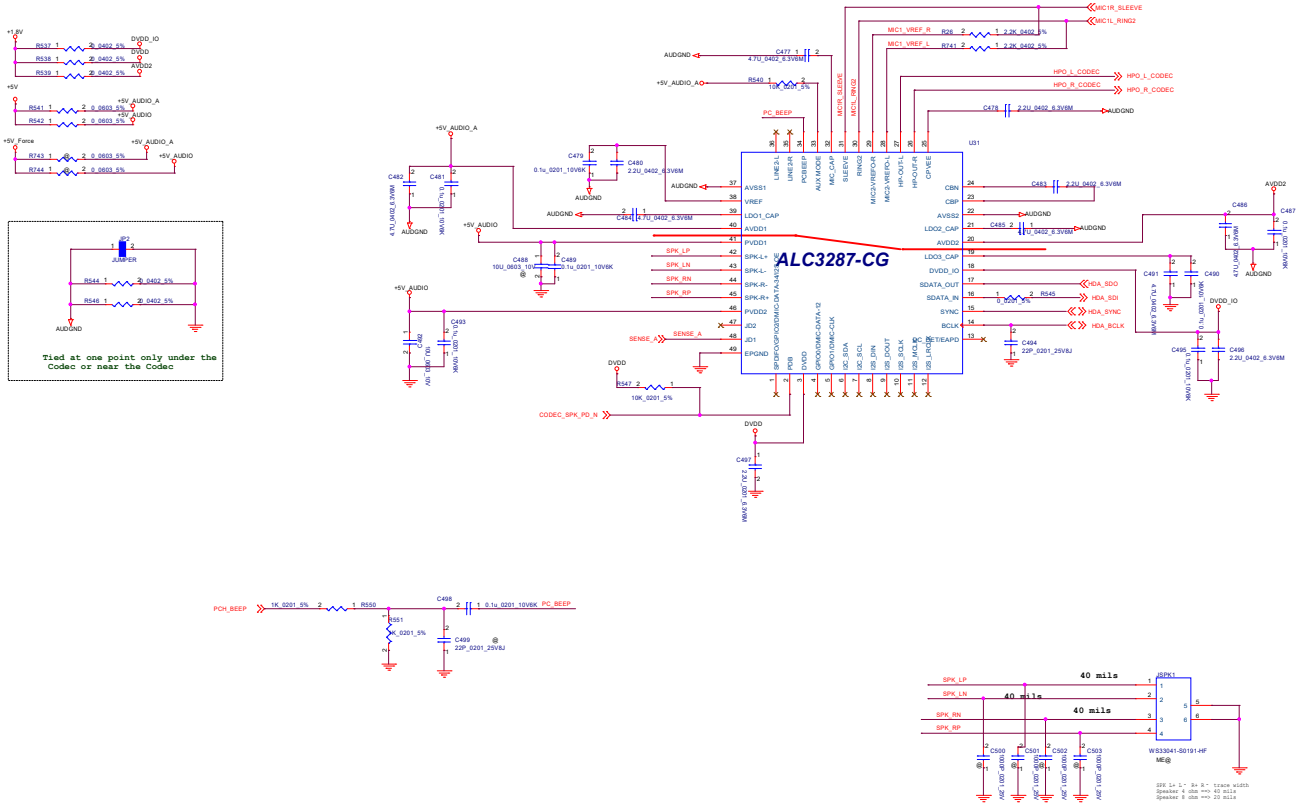

lenovo 联想	LENOVO.CRDN	
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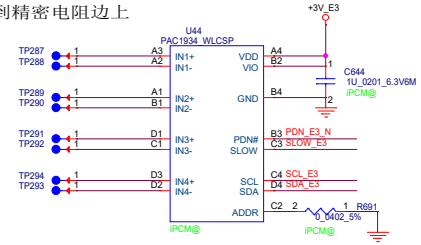
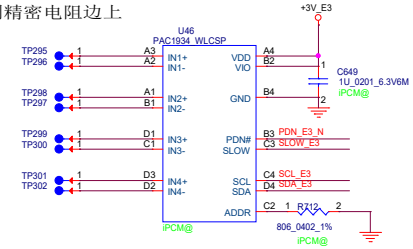
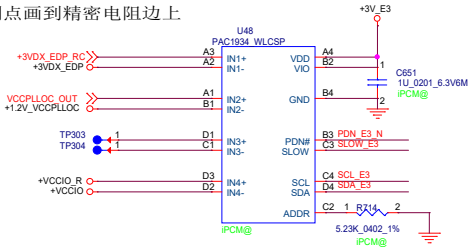
测点画到精密电阻边上



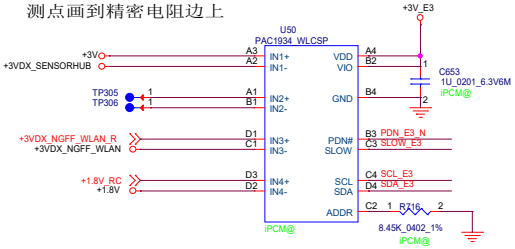
测点画到精密电阻边上



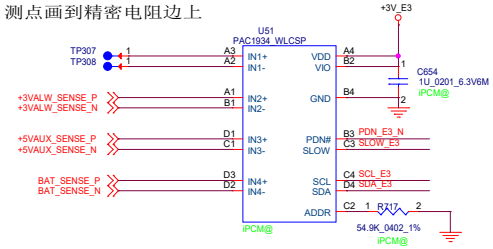
测点画到精密电阻边上



测点画到精密电阻边上

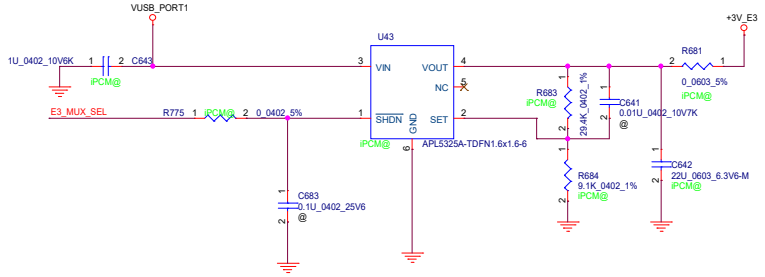


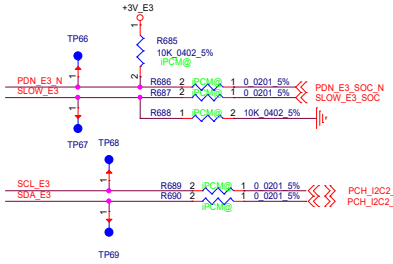
测点画到精密电阻边上

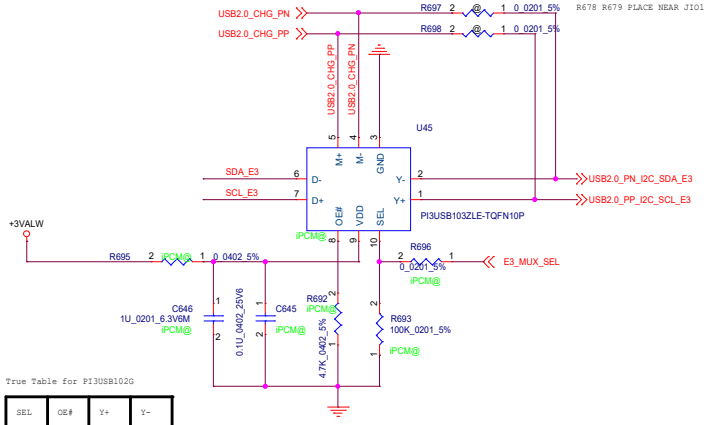


ADDR电阻：

0 ohm	0010_000
499 ohm	0010_001
806 ohm	0010_010
1.27K ohm	0010_011
2.05k ohm	0010_100
3.24k ohm	0010_101
5.23k ohm	0010_110
8.45k ohm	0010_111
21.5k ohm	0011_001
54.9k ohm	0011_011







True Table for PI3USB102G

SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

lenovo联想 LENOVO.CRDN

Title: iPCM

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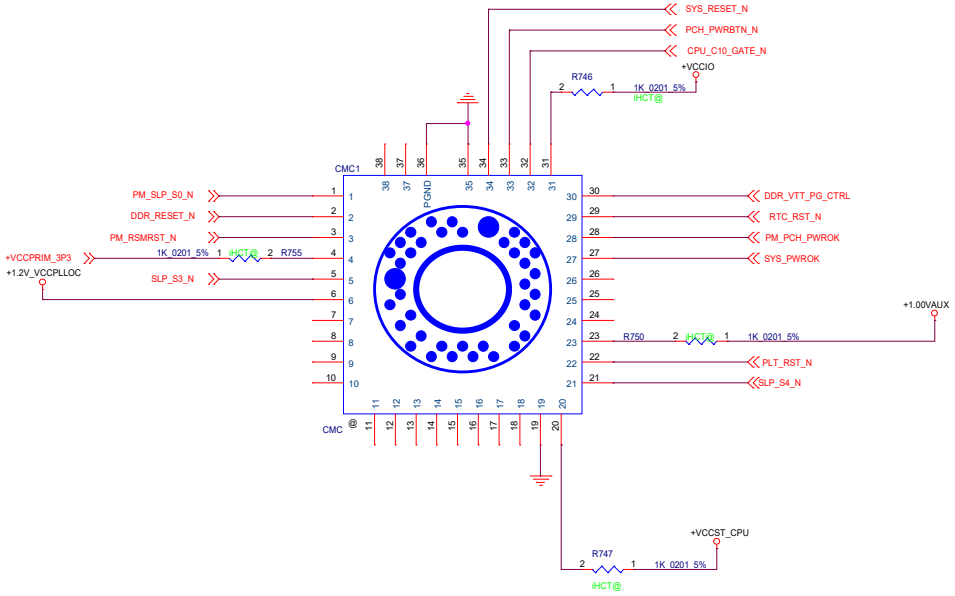

CAD NOTE:
R746,R747,R748,R749,R750,R751,R752,R753,R754,R755 CLOSE TO POWER SOURCE

lenovo联想	LENOVO.CRDN	
Title: iHCT		
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lenovo联想 LENOVO.CRDN

Title: BLANK

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Title: BLANK

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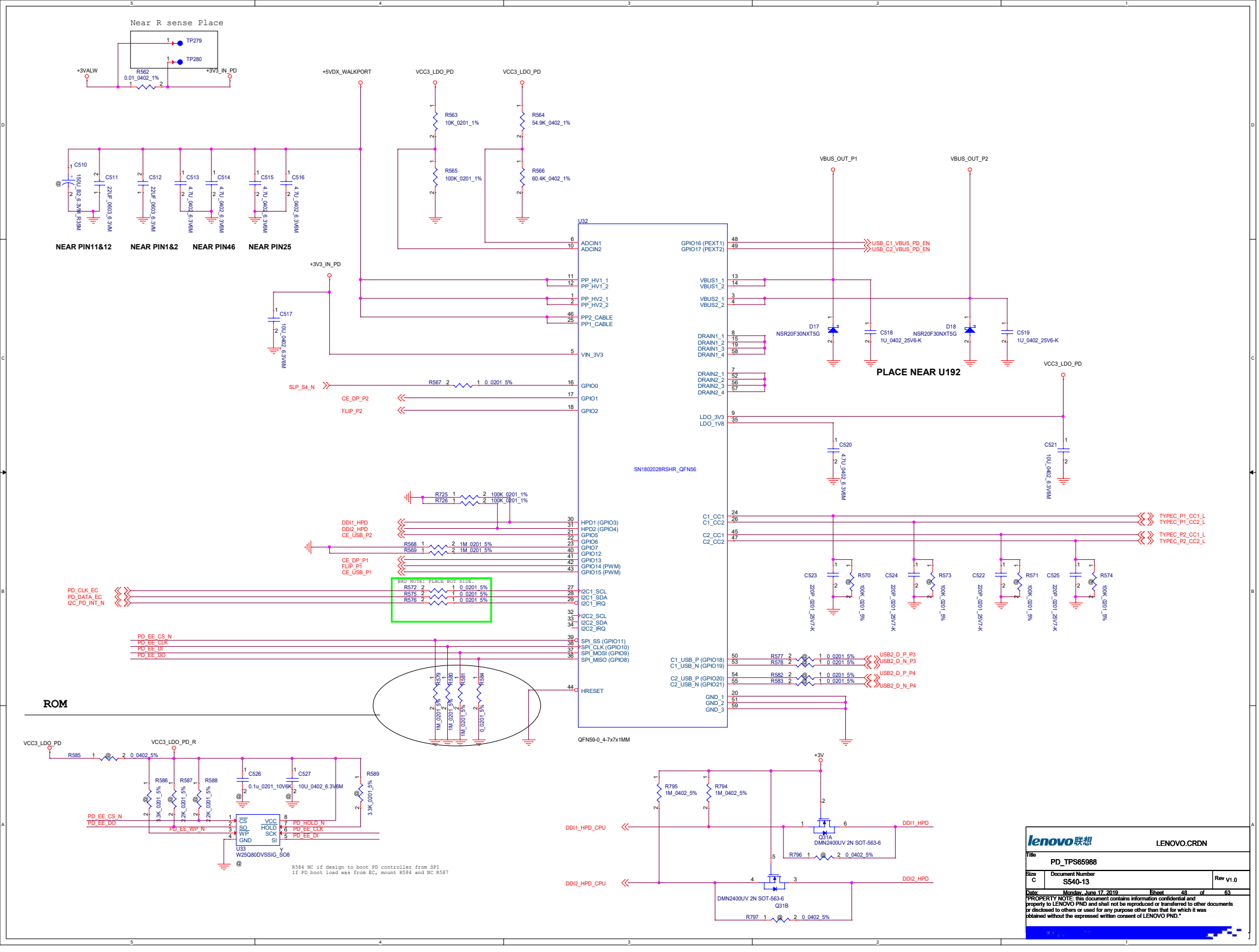

lenovo联想 LENOVO.CRDN

Title: PD_TPS65988

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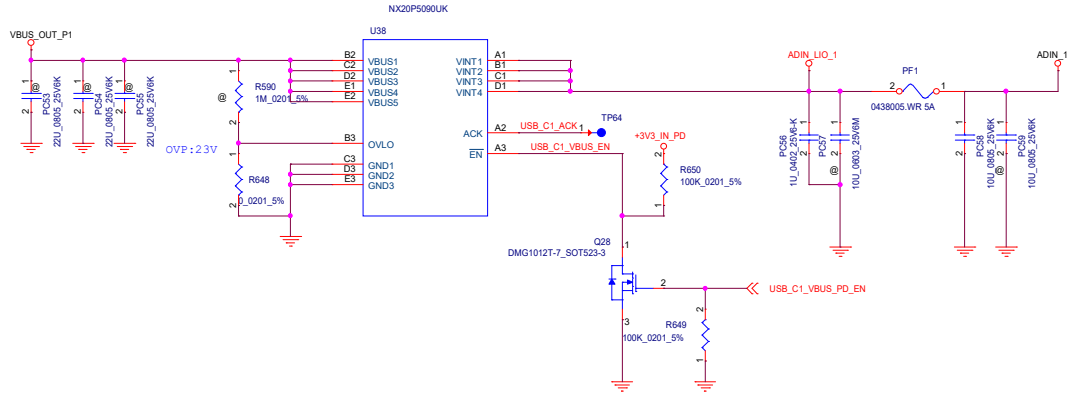
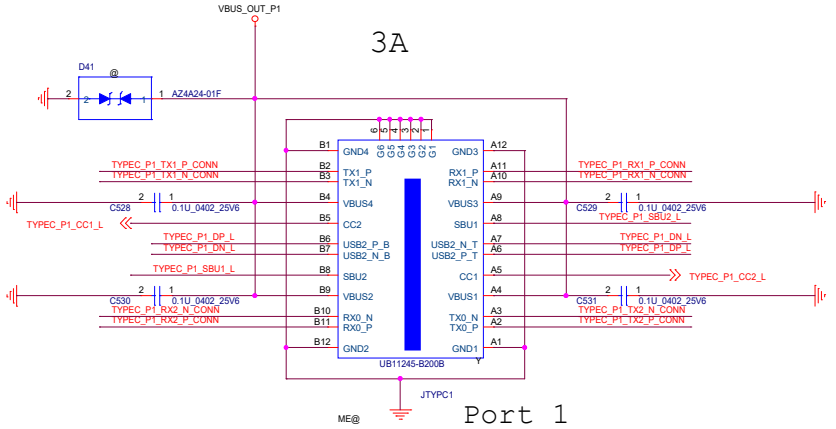
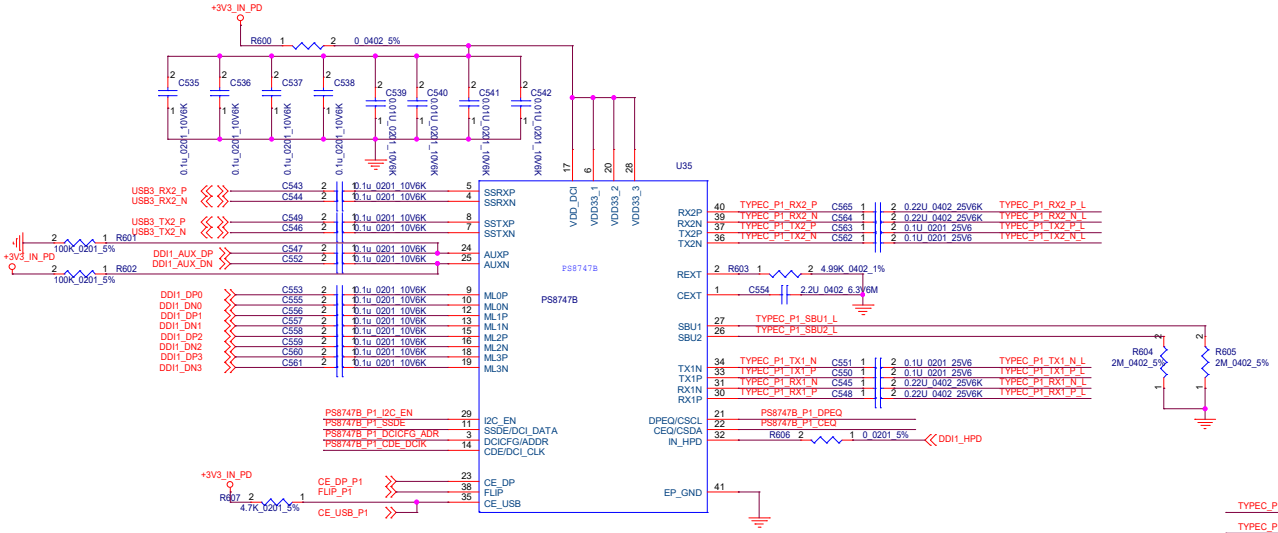
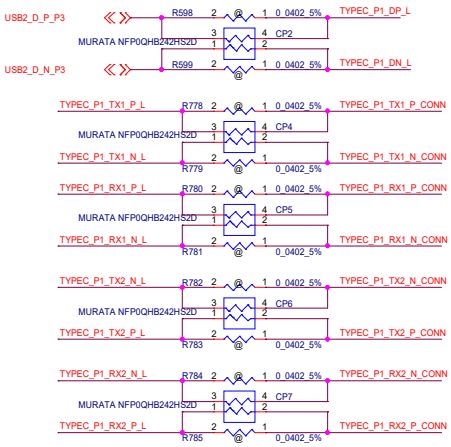
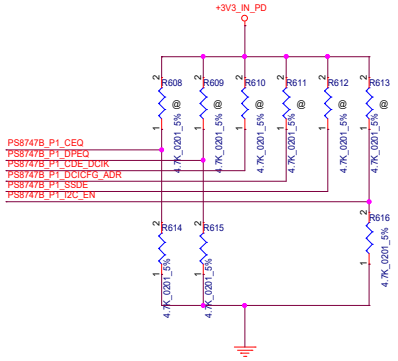
Type C PORT A VBUS SWITCH

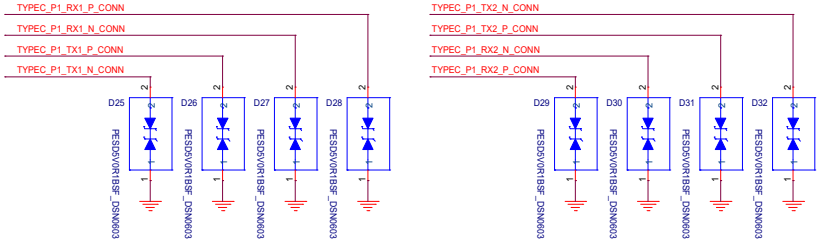


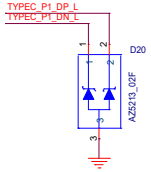


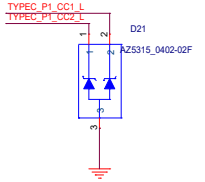


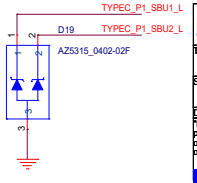












lenovo联想		LENOVO.CRDN	
Title	TYPEC_PORTA		
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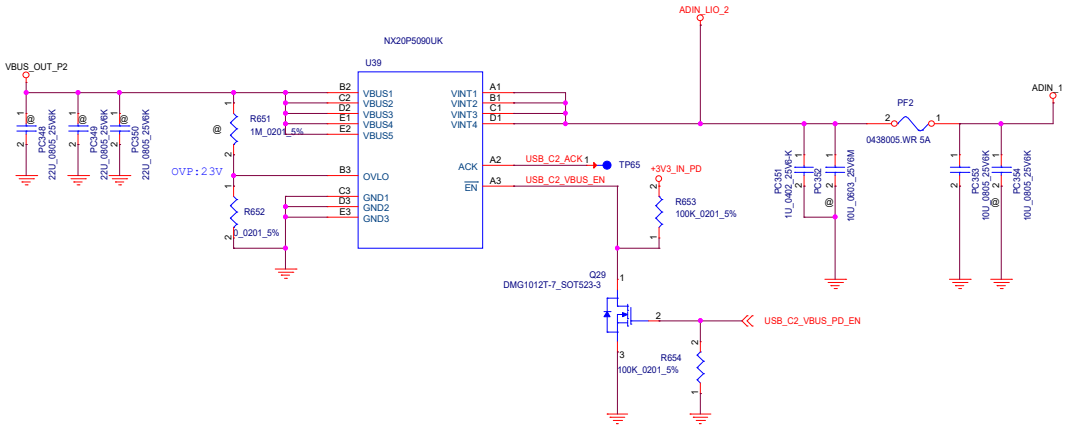
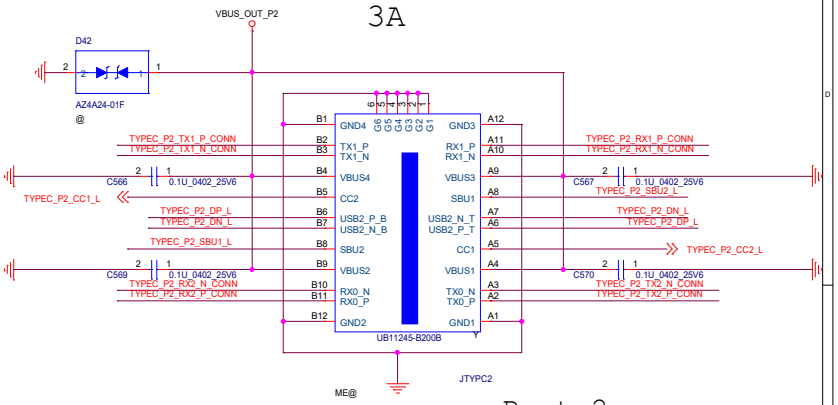
Type C PORT B VBUS SWITCH





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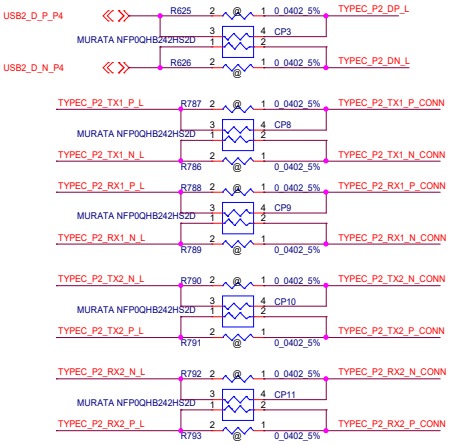

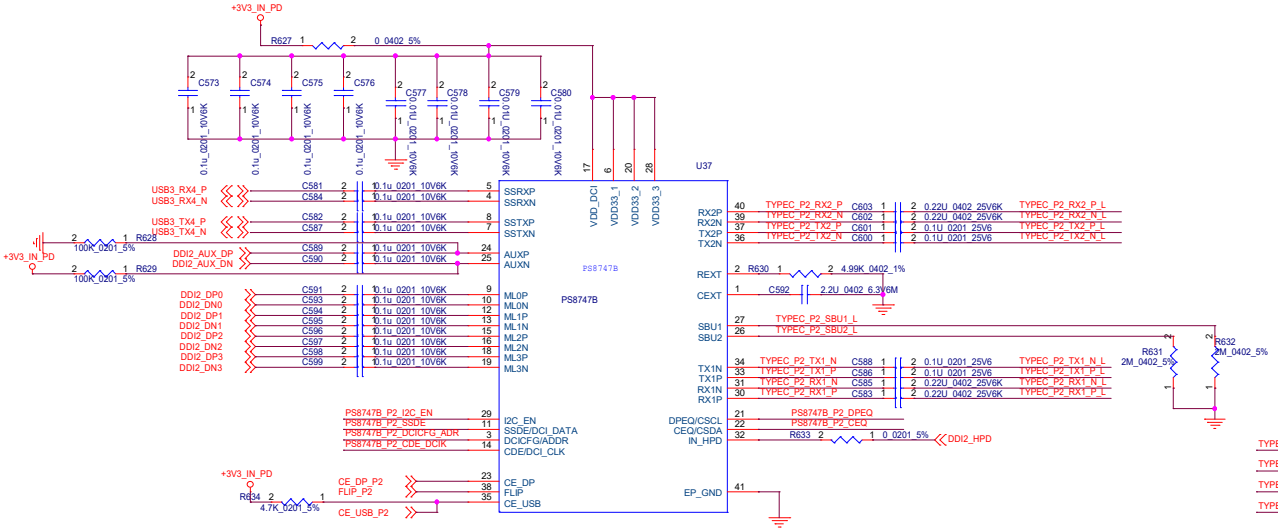

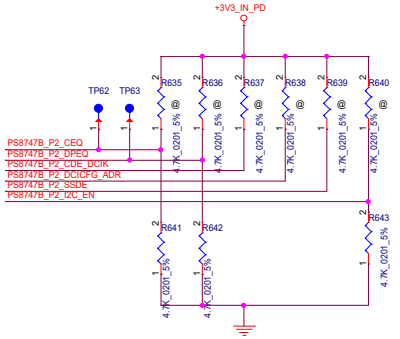

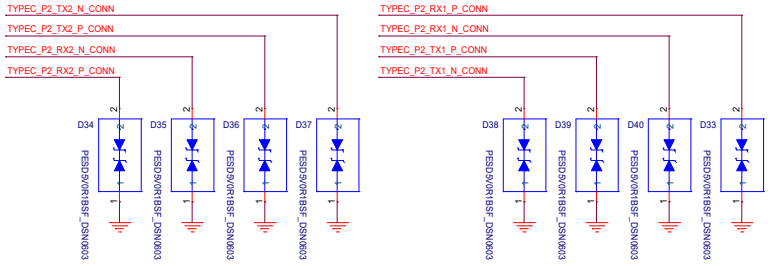

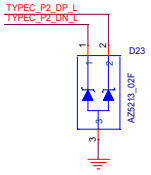

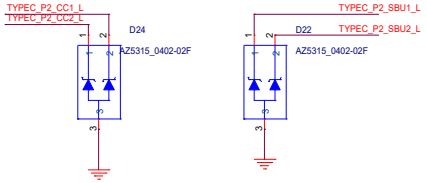

lenovo联想	LENOVO.CRDN	
Title: TYPEC_PORTB		
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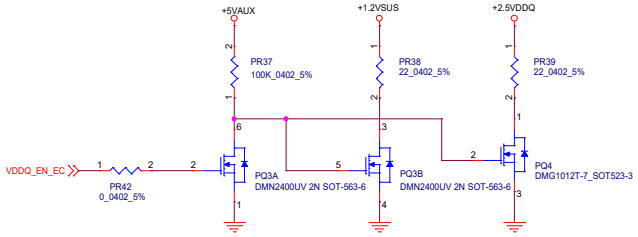

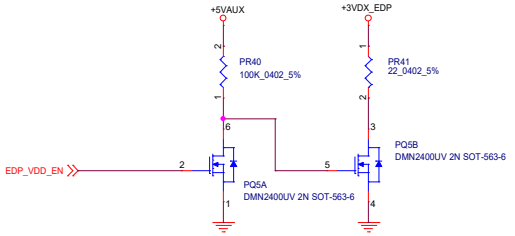

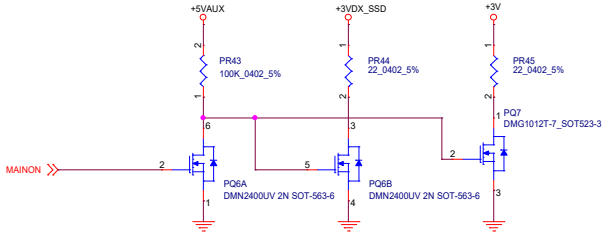

lenovo联想 LENOVO.CRDN

Title: DISCHARGE

Size	Document Number	Rev
C	S540-13	V1.0

Date: Monday, June 17, 2019 Sheet 51 of 63

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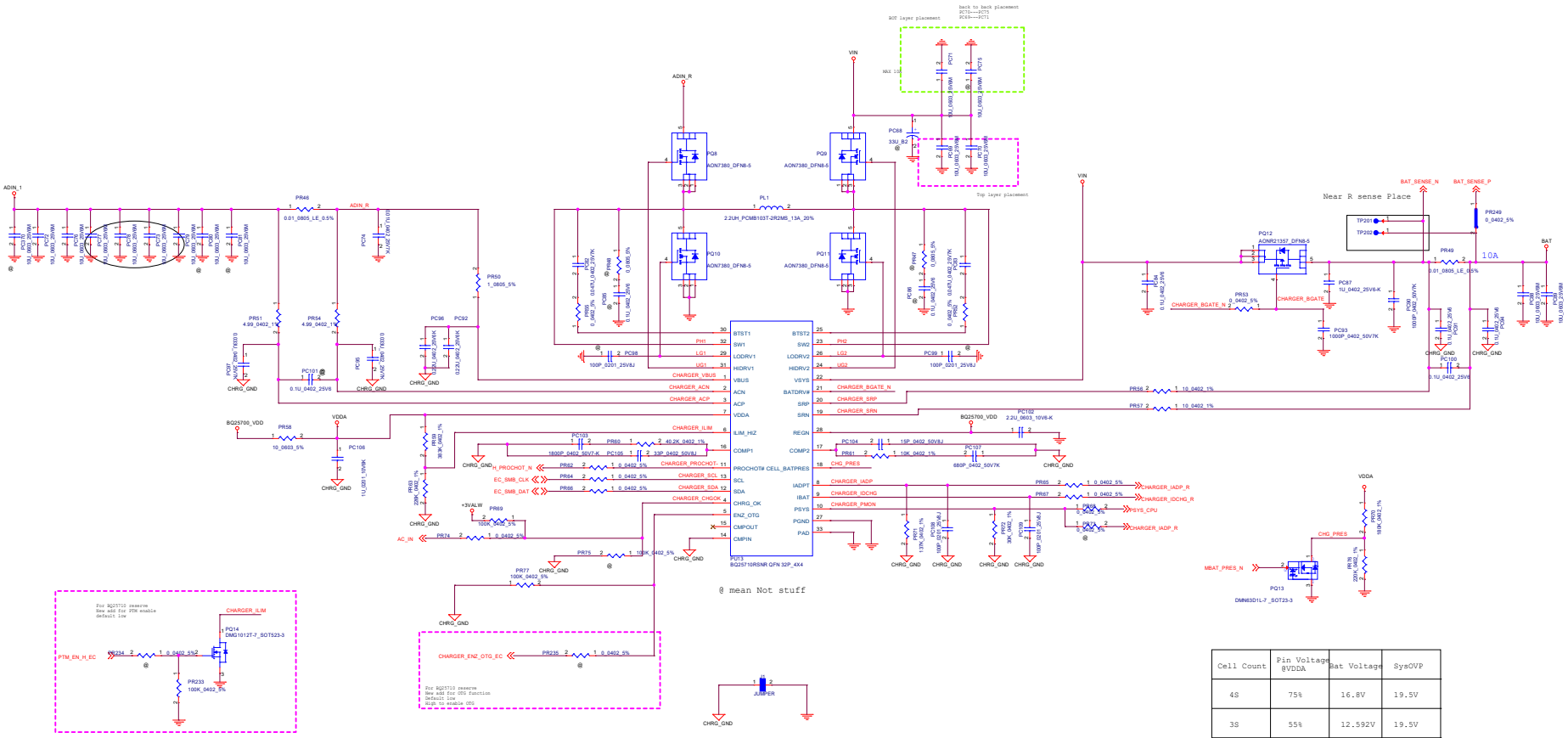

Cell Count	Pin Voltage @VDDA	Bat Voltage	SysOVP
4S	75%	16.8V	19.5V
3S	55%	12.592V	19.5V
2S	40%	8.4V	12V
1S	25%	4.192V	5V

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Title: NVDC CHARGER

Size: D | Document Number: S540-13 | Rev: V1.0

Date: Monday, June 17, 2019 | Sheet 52 of 63

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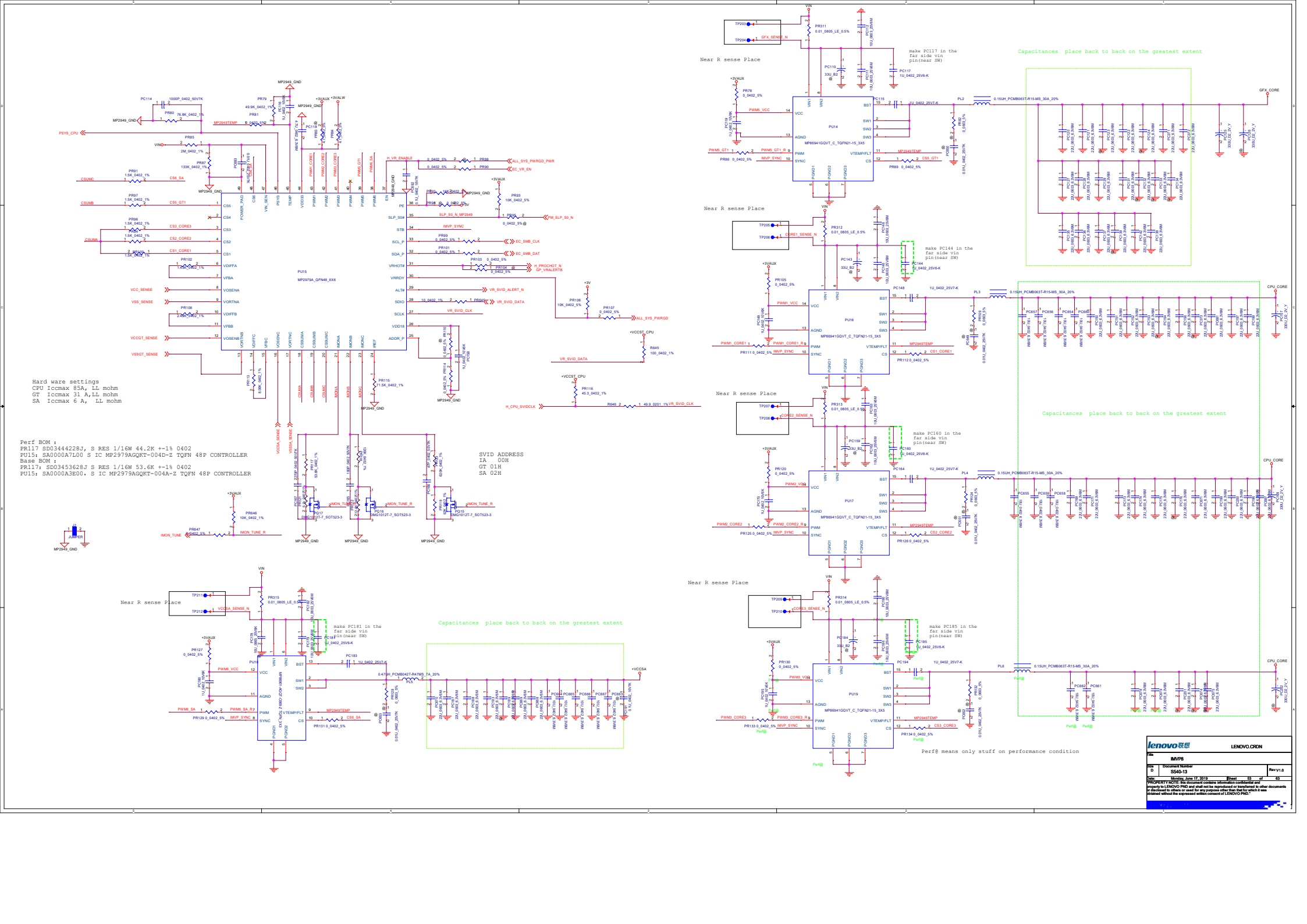
Hard ware settings
CPU Iccmax 85A, LL mohm
GT Iccmax 31 A,LL mohm
SA Iccmax 6 A, LL mohm
Perf BOM :
PR117 SD03444228J, S RES 1/16W 44.2K +-1% 0402
PU15: SA0000A7L00 S IC MP2979AGQKT-004D-Z TQFN 48P CONTROLLER
Base BOM :
PR117: SD03453628J S RES 1/16W 53.6K +-1% 0402
PU15: SA0000A3E00, S IC MP2979AGQKT-004A-Z TQFN 48P CONTROLLER
SVID ADDRESS
IA 00H
GT 01H
SA 02H
Near R sense Place
make PC117 in the far side vin pin(near SW)
make PC144 in the far side vin pin(near SW)
make PC160 in the far side vin pin(near SW)
make PC181 in the far side vin pin(near SW)
make PC185 in the far side vin pin(near SW)
Capacitances place back to back on the greatest extent
Perf@ means only stuff on performance condition
MP2949_GND
+3VAUX
+3VALW
VIN
+VCCSA
+VCCST_CPU
+3V
GFX_CORE
CPU_CORE
PU14
PU16
PU17
PU19
PU15
MP88941GQVT_C_TQFN21-15_5X5
MP2979A_QFN48_6X6
LENOVO.CRDN
IMVP8
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63
LENOVO CONFIDENTIAL
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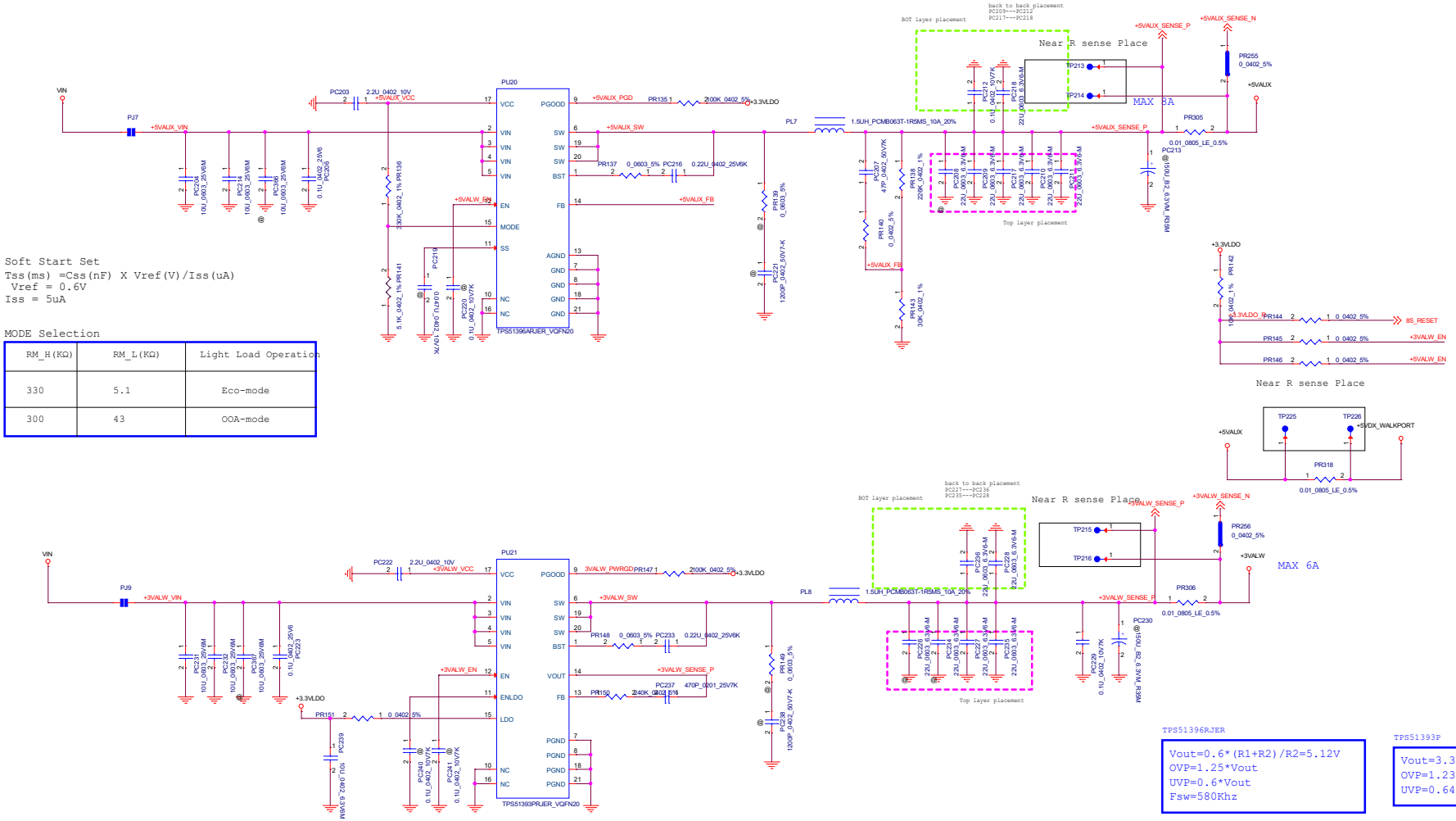

lenovo联想	LENOVO.CRDN		
Title	+3VALW/+5VAUX		
Size: Custom	Document Number: S540-13	Rev: V1.0	
Date: Monday, June 17, 2019	Sheet 54 of 63		

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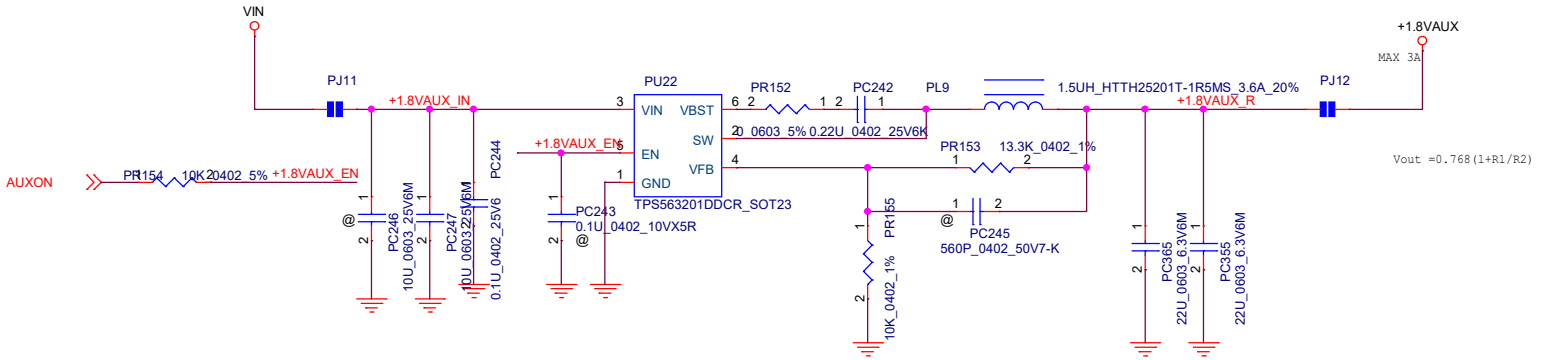
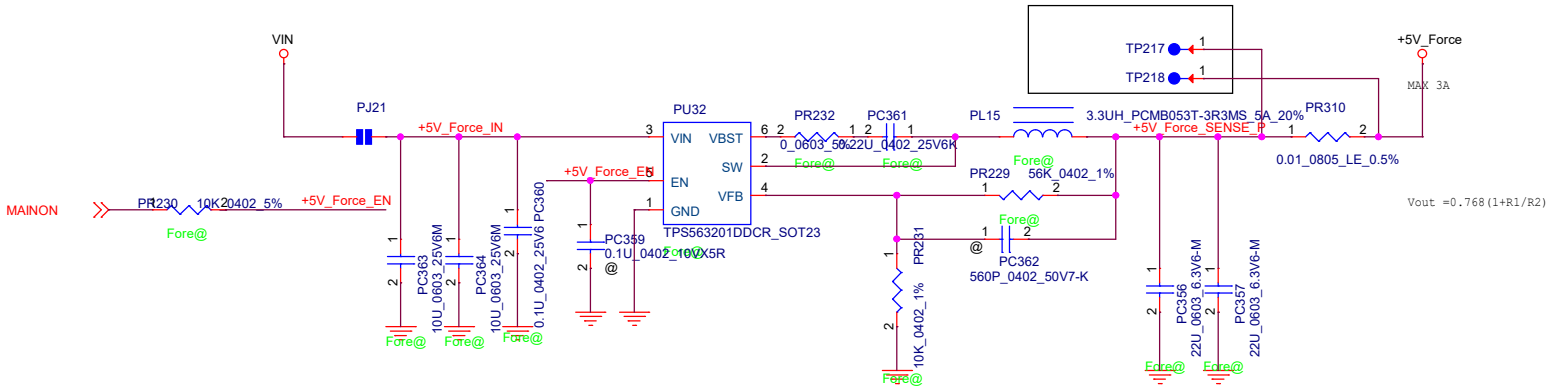


Near R sense Place



Option For Foretouch function
Force@ Only Stuff On forcetouch Existence

lenovo联想 LENOVO.CRDN

Title: P55--PWR_+1.8VAUX/+5V_Force

Size	Document Number	Rev
B	S540-13	V1.0

Date: Monday, June 17, 2019 Sheet 55 of 63

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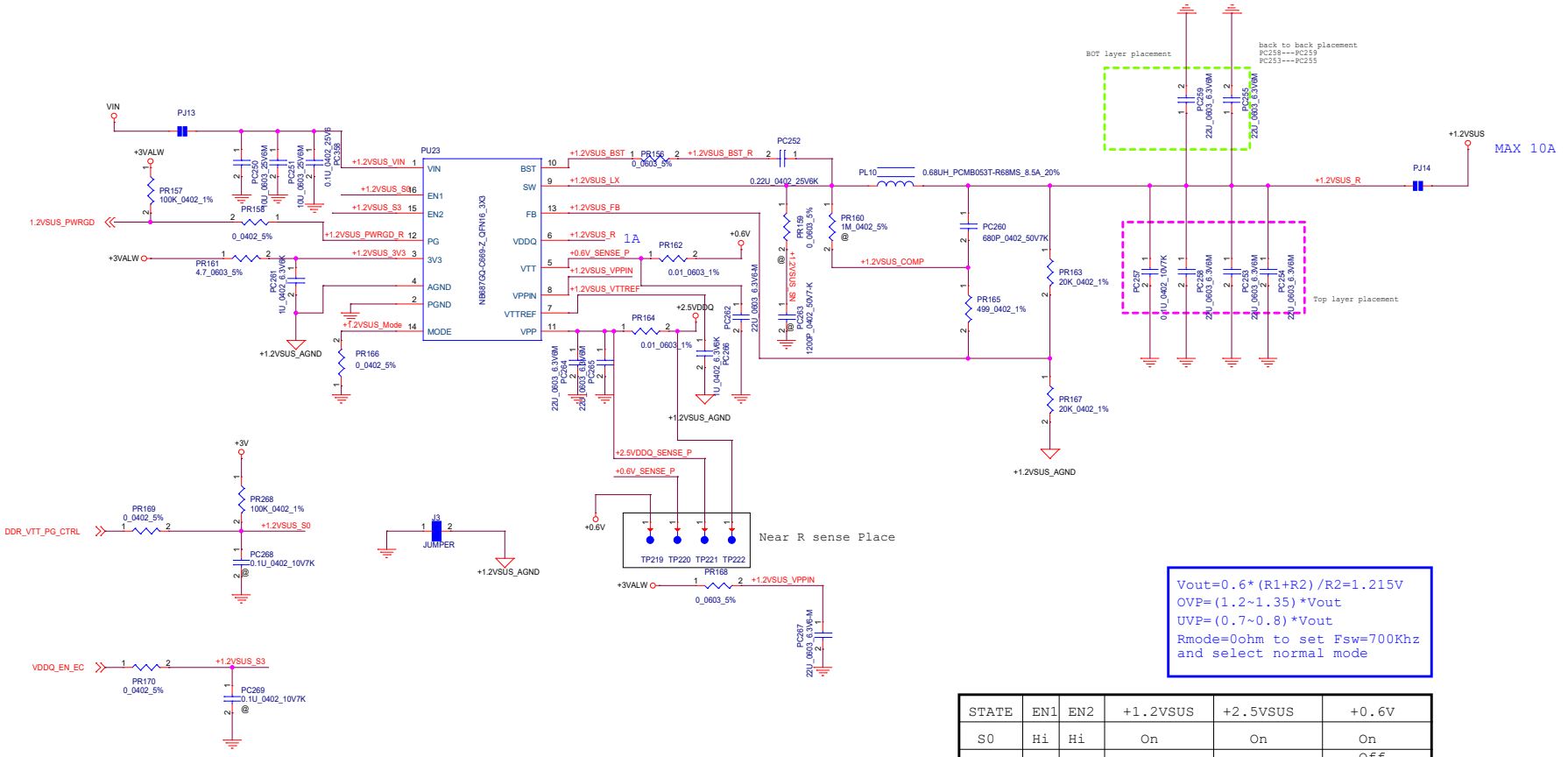

Vout=0.6*(R1+R2)/R2=1.215V
OVP=(1.2~1.35)*Vout
UVP=(0.7~0.8)*Vout
Rmode=0ohm to set Fsw=700Khz and select normal mode

STATE	EN1	EN2	+1.2VSUS	+2.5VSUS	+0.6V
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

lenovo联想	LENOVO.CRDN	
Title	+1.2VSUS/+0.6V	
Size C	Document Number S540-13	Rev V1.0
Date: Monday, June 17, 2019	Sheet 56 of 63	

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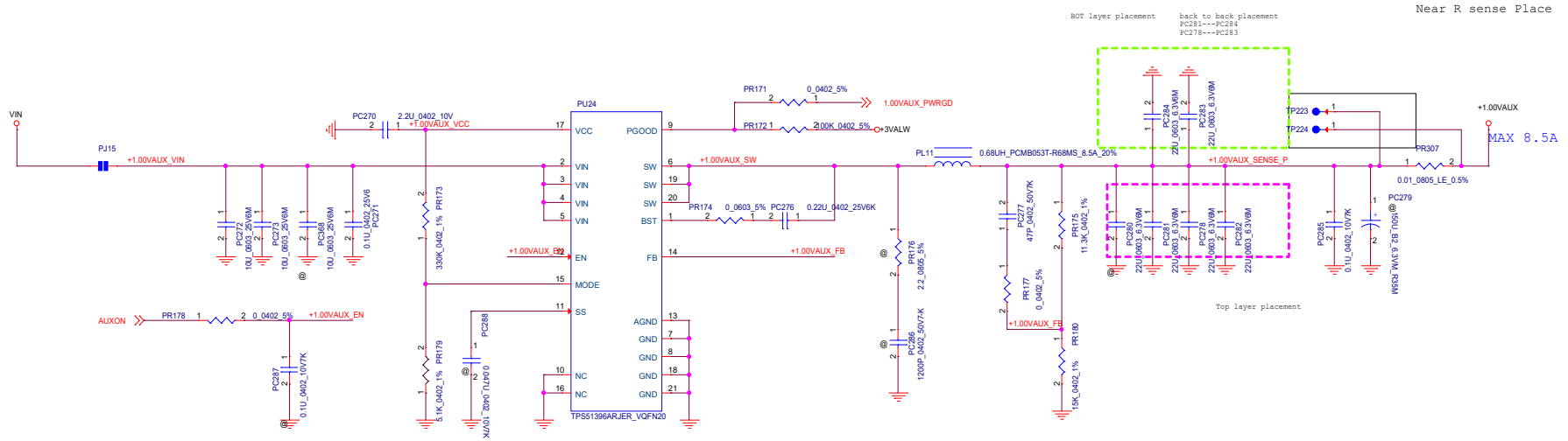

Soft Start Set

Tss(ms) =Css(nF) X Vref(V)/Iss(uA)

Vref = 0.6V

Iss = 5uA

MODE Selection

RM_H(KΩ)	RM_L(KΩ)	Light Load Operation
330	5.1	Eco-mode
300	43	OOA-mode

Vout=0.6*(R1+R2)/R2=1.052V

OVP=1.25*Vout

UVP=0.6*Vout

Fsw=580Khz

lenovo联想 LENOVO.CRDN

Title: PWR_+1.00VAUX

Size: C | Document Number: S540-13 | Rev V1.0

Date: Monday, June 17, 2019 | Sheet 57 of 63

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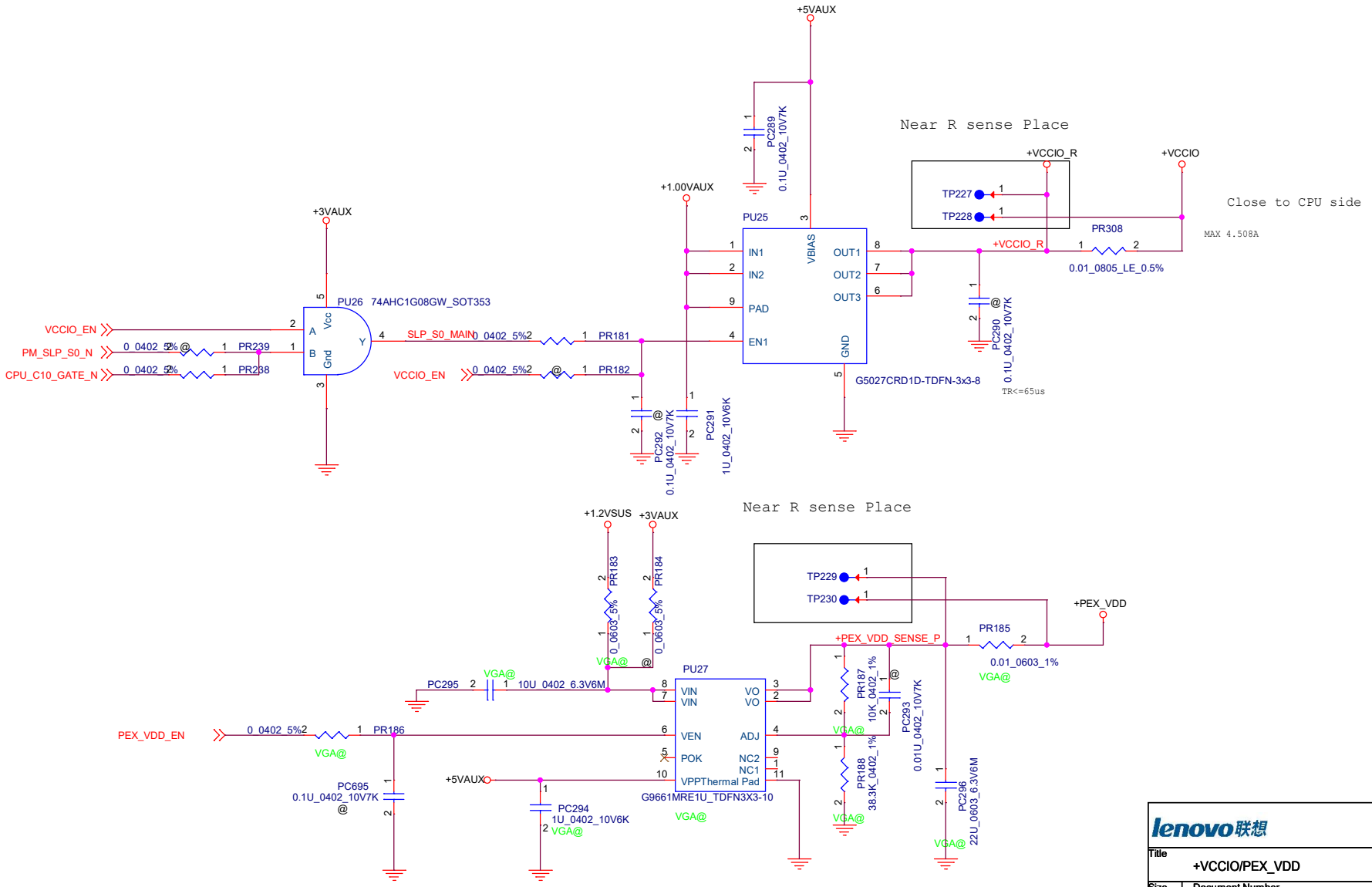

lenovo联想	LENOVO.CRDN	
Title: +VCCIO/PEX_VDD		
Size: B	Document Number: S540-13	Rev: V1.0
Date: Monday, June 17, 2019	Sheet 58 of 63	

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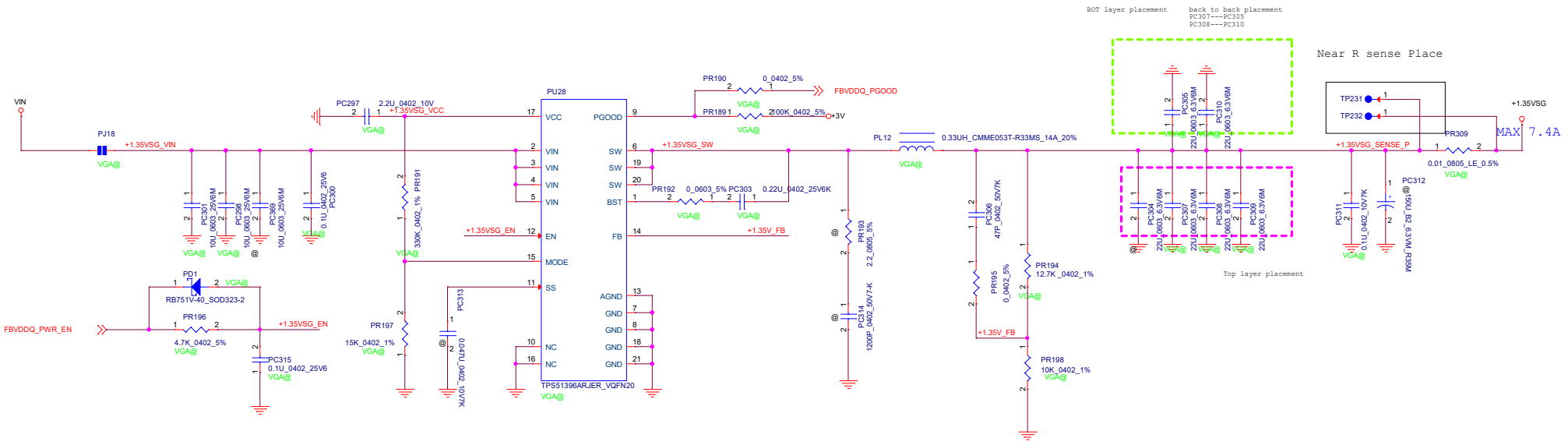

Soft Start Set

Tss(ms) =Css(nF) X Vref(V)/Iss(uA)
Vref = 0.6V
Iss = 5uA

MODE Selection

RM_H(KΩ)	RM_L(KΩ)	Light Load Operation
330	5.1	Eco-mode
300	43	OOA-mode

VGA@ Only Stuff On DGPU Existence

Vout=0.6*(R1+R2)/R2=1.38V
OVP=1.25*Vout
UVP=0.6*Vout
Fsw=580Khz

lenovo联想 LENOVO.CRDN

Title: +1.35VGS

Size: Custom | Document Number: S540-13 | Rev V1.0

Date: Monday, June 17, 2019 | Sheet 59 of 63

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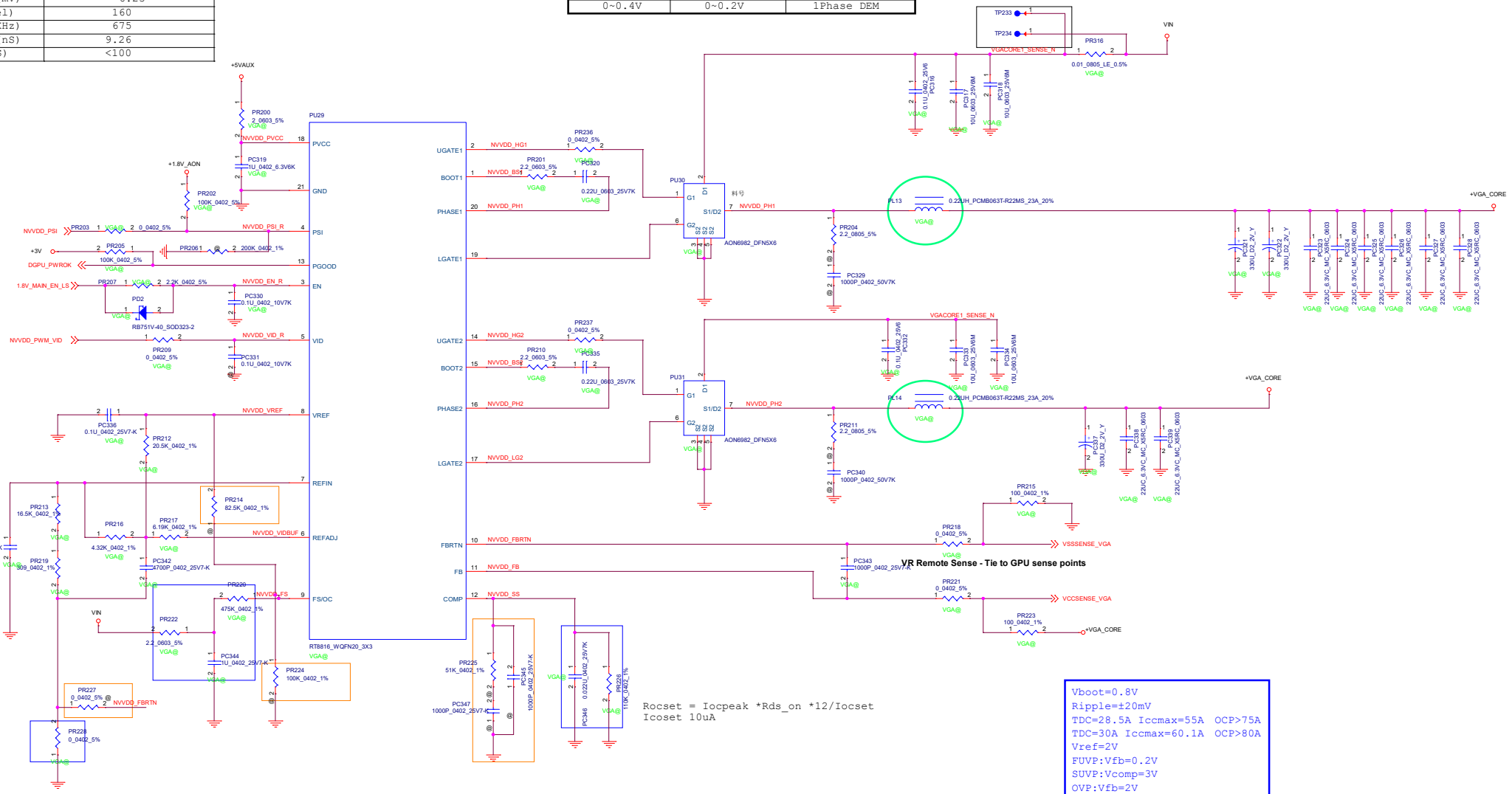
PWM-VID Specification	
	N17 Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
N(level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM

Near R sense Place



lenovo联想	LENOVO.CRDN
Title	+VGA_CORE
Size: Custom	Document Number: S540-13
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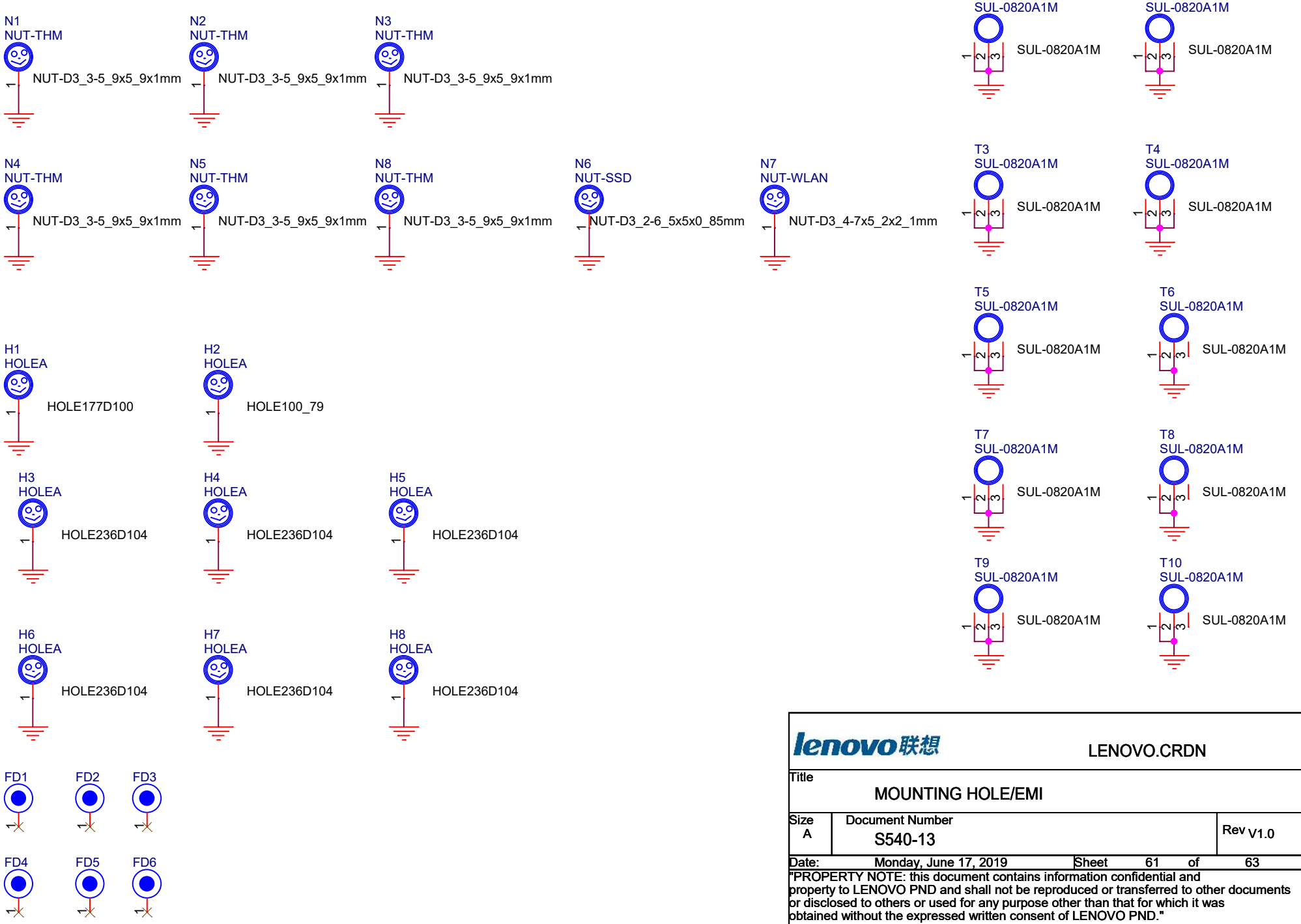

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Title

MOUNTING HOLE/EMI

Size	Document Number	Rev
A	S540-13	V1.0

Date: Monday, June 17, 2019 Sheet 61 of 63

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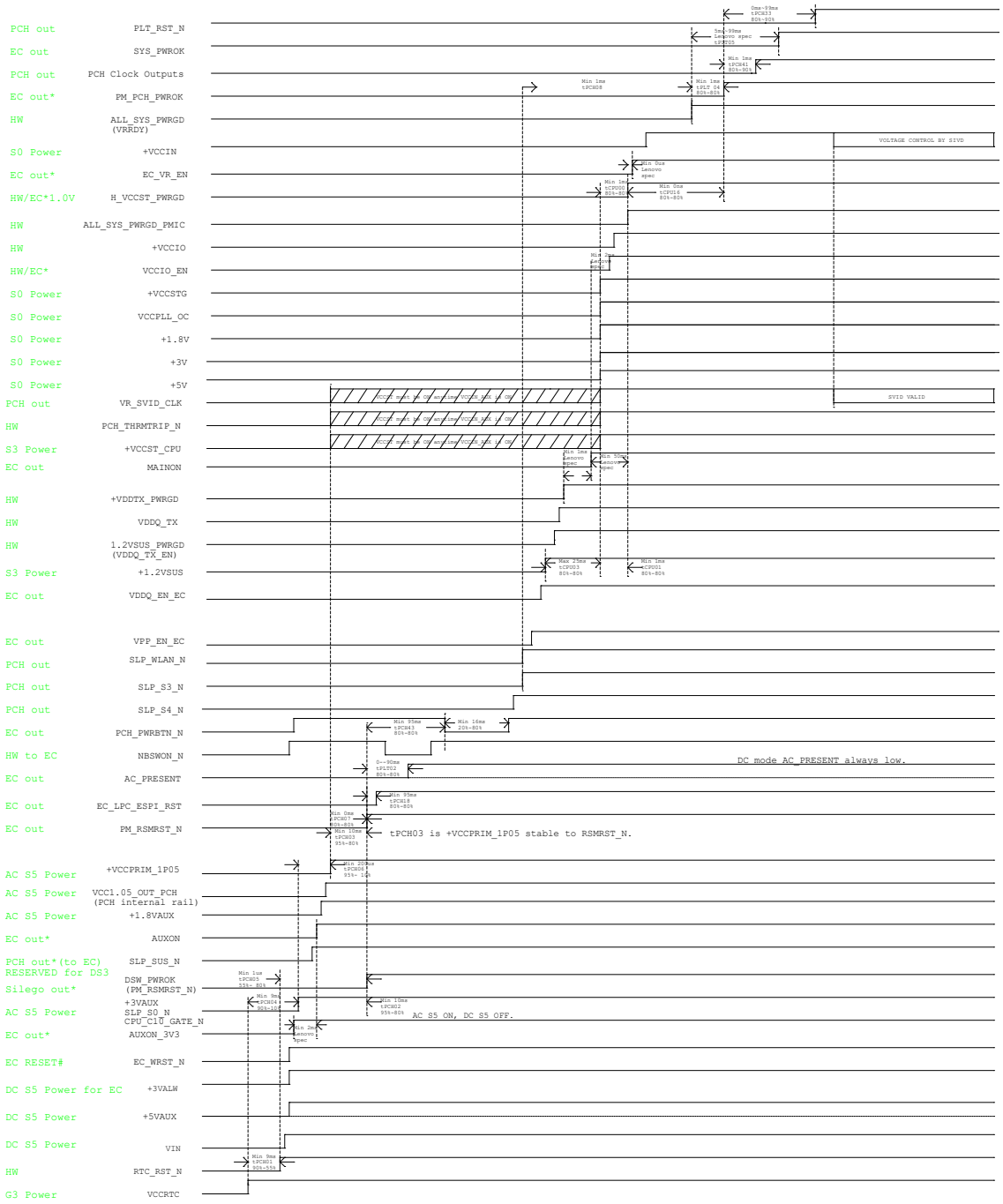
G3

AC/DC mode S5/S4 to S0 (Non Deep Sx)



G3

AC/DC mode S5/S4 to S0 (Non Deep Sx platform)

lenovo	LENOVO.CRDN		
Title	CML Power Sequence		
Size	Document Number		Rev V1.0
C	8540-13		
Date: Monday, May 04, 2020	Sheet 46 of 55		

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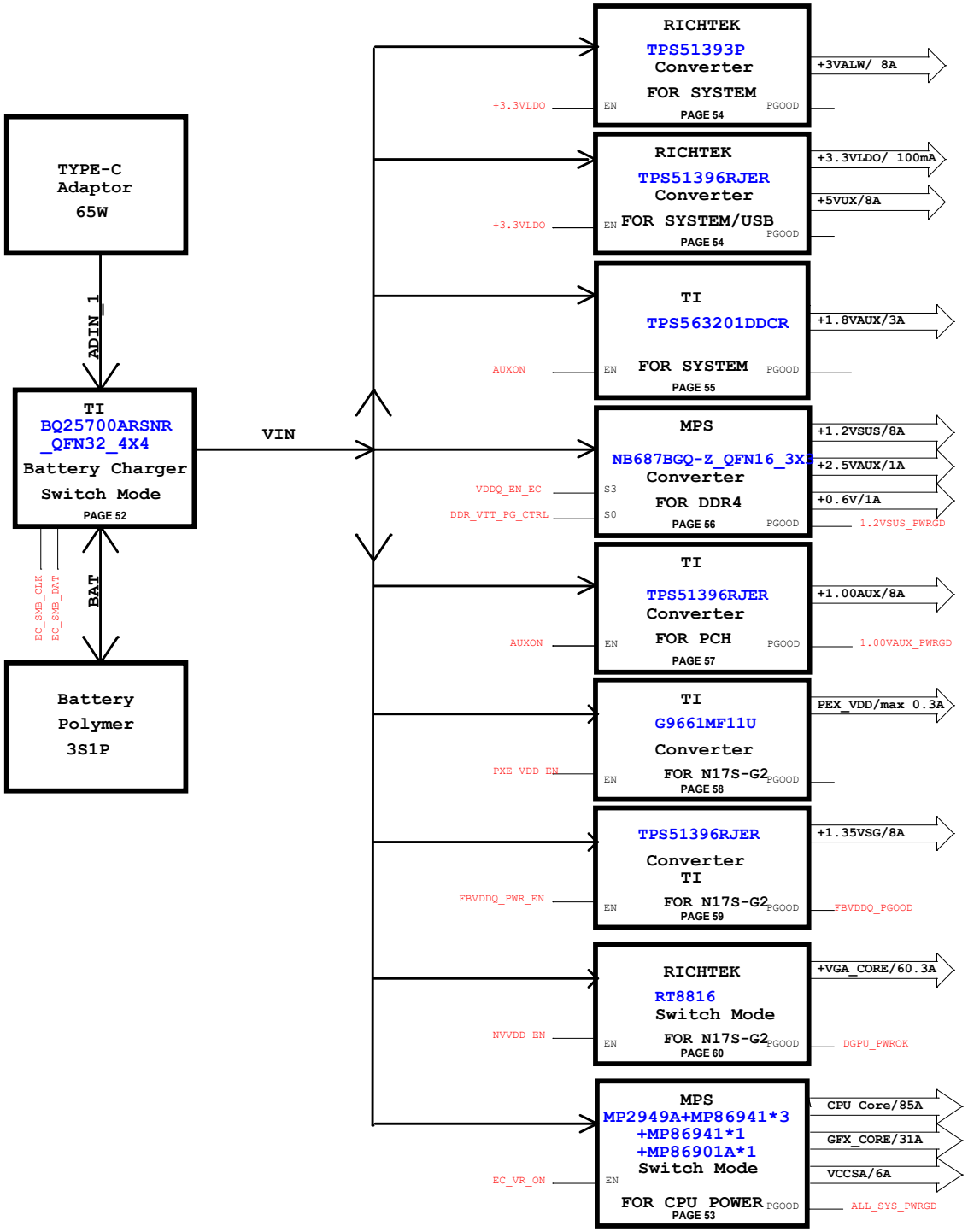

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Title: PWR-Power Diagram

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